Secure Computation with Sublinear Cost

Mike Rosulek

Oregon State University OSU

Collaborators: Arash Afshar / Zhangxiang Hu / Payman Mohassel

Secure 2-party computation

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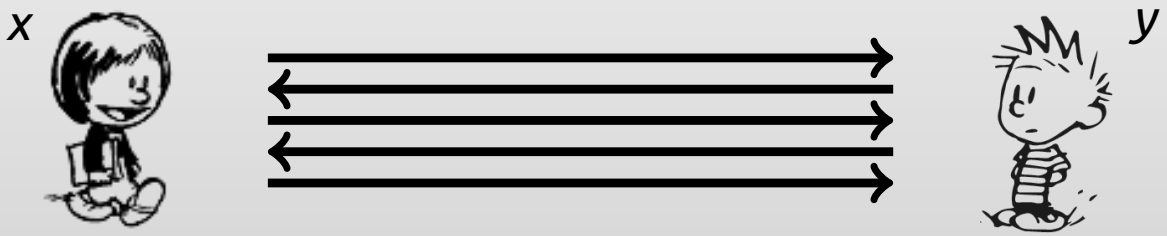

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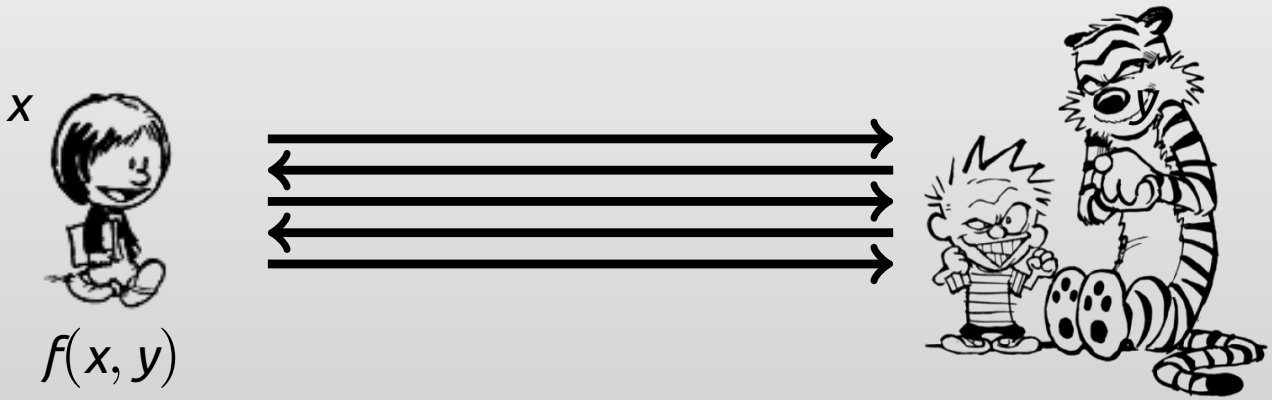

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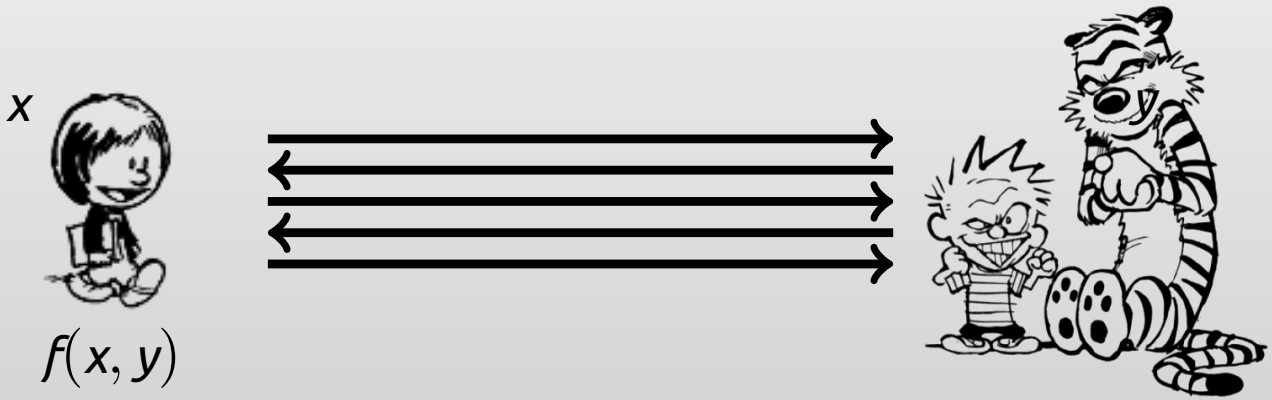

Examples:

- Run proprietary classifier x on private data y
- Evaluate statistics on combined medical records x & y
- . . .

Fundamental Limits

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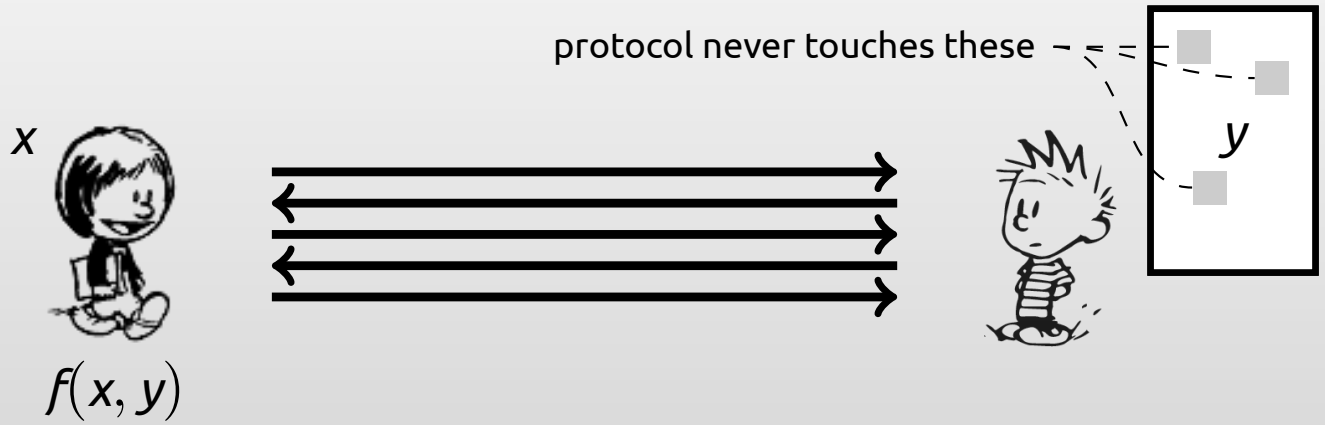

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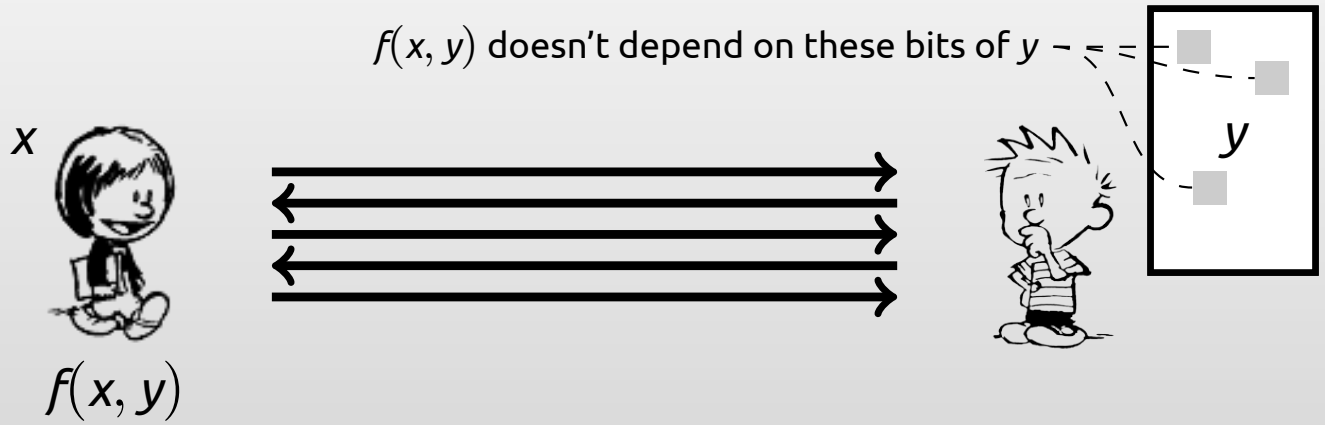

Example:

- $y =$ genetic database
- $x =$ DNA markers
- $f(x, y) =$ diagnosis

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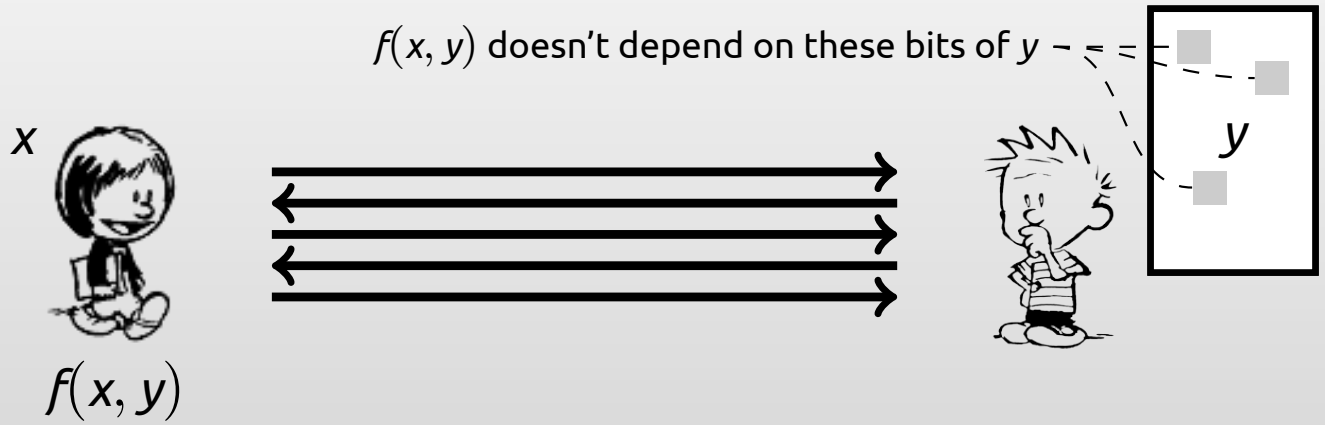

Example:

- $y =$ genetic database
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$\Rightarrow$ **in general**, security demands that all of the data is touched

Limits of Standard Techniques

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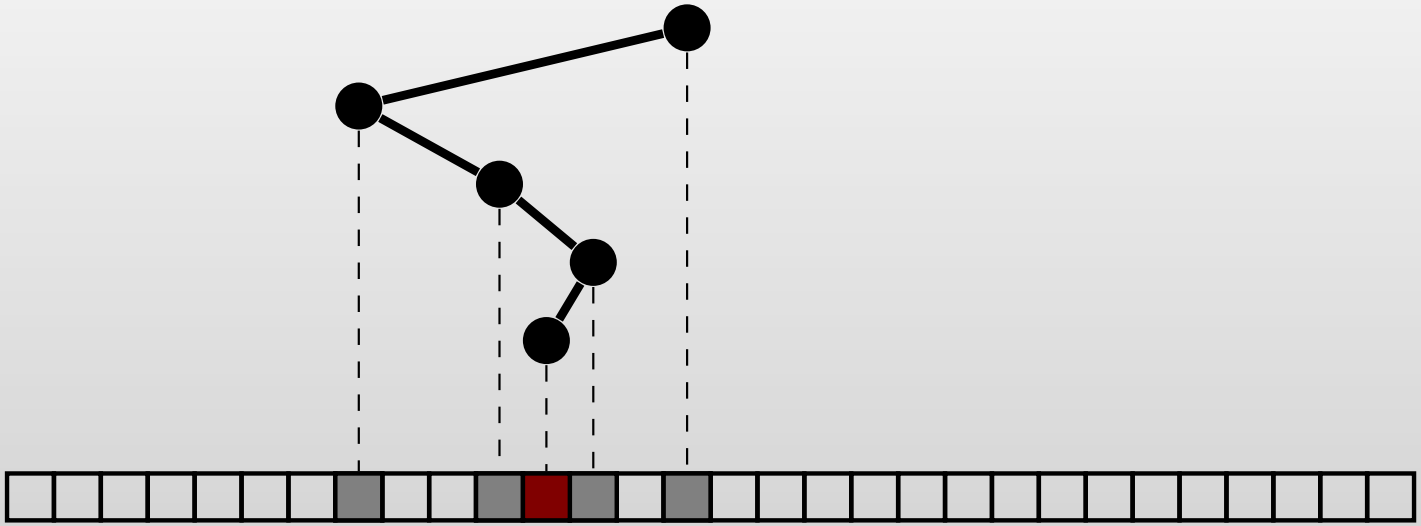

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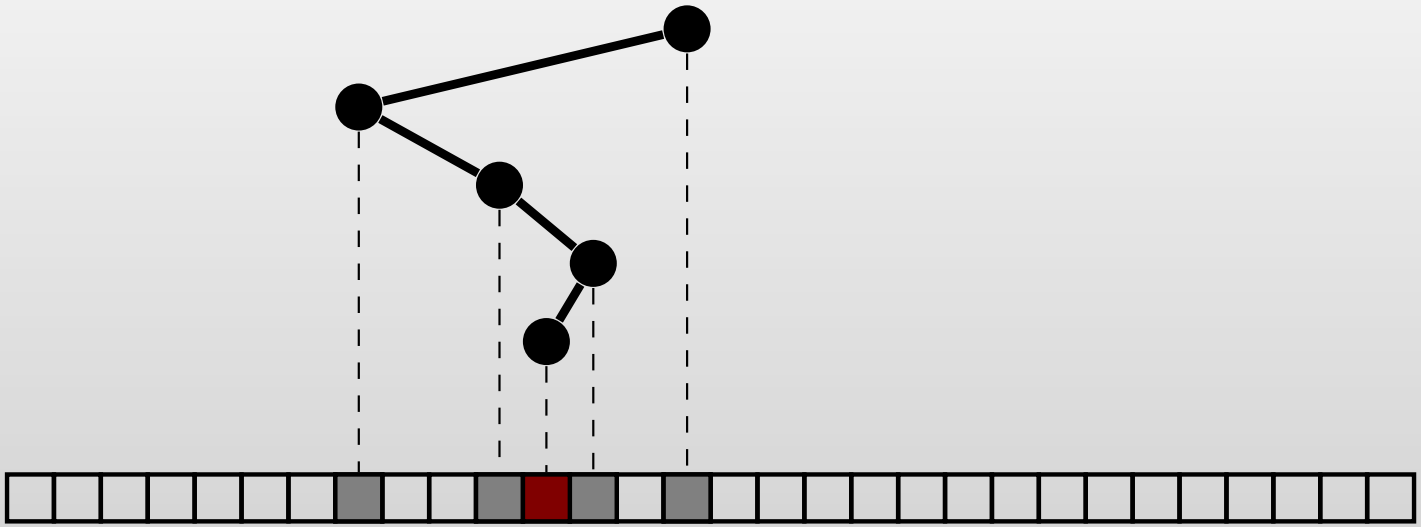

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first express f as a boolean circuit,
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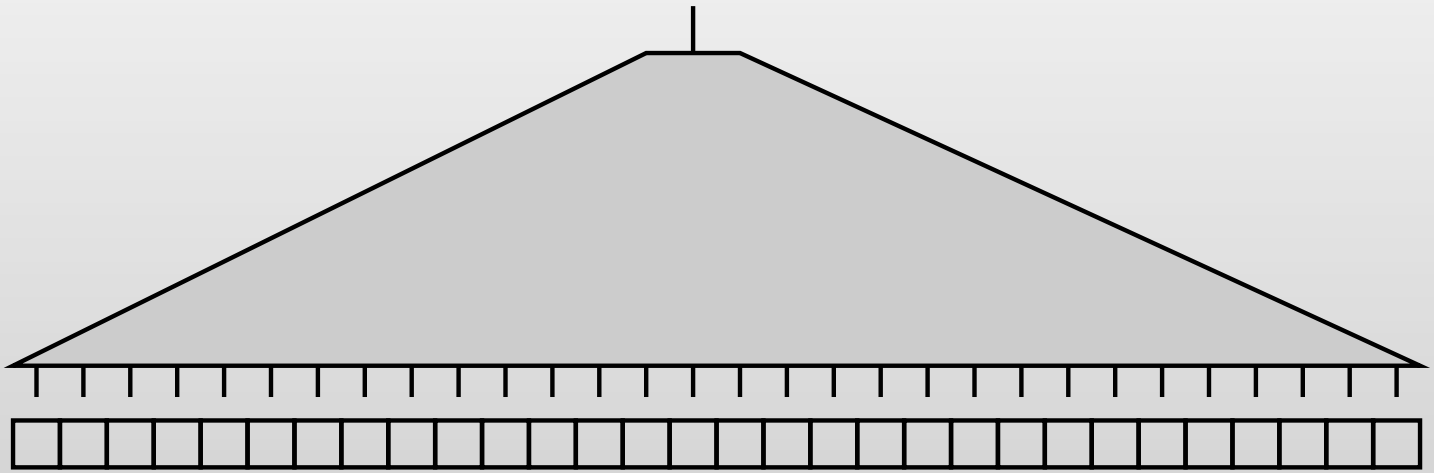

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2. General-purpose 2PC scales with size of **circuit representation**, which is always at least linear in input size.

In this talk:

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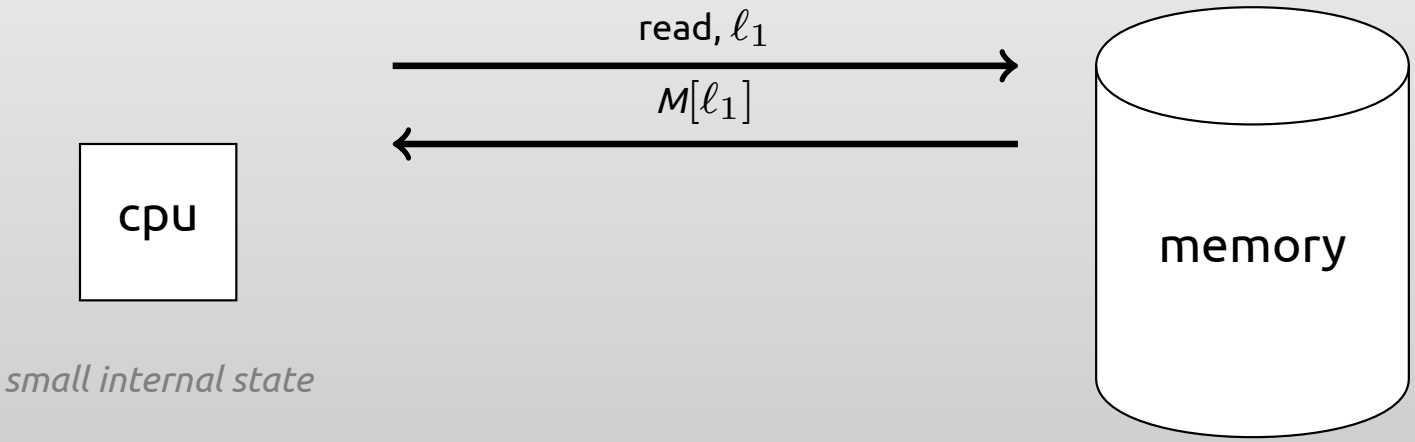
2. Protocol must “touch every bit”, but amortize this cost across many executions.

RAM programs

small internal state

RAM programs



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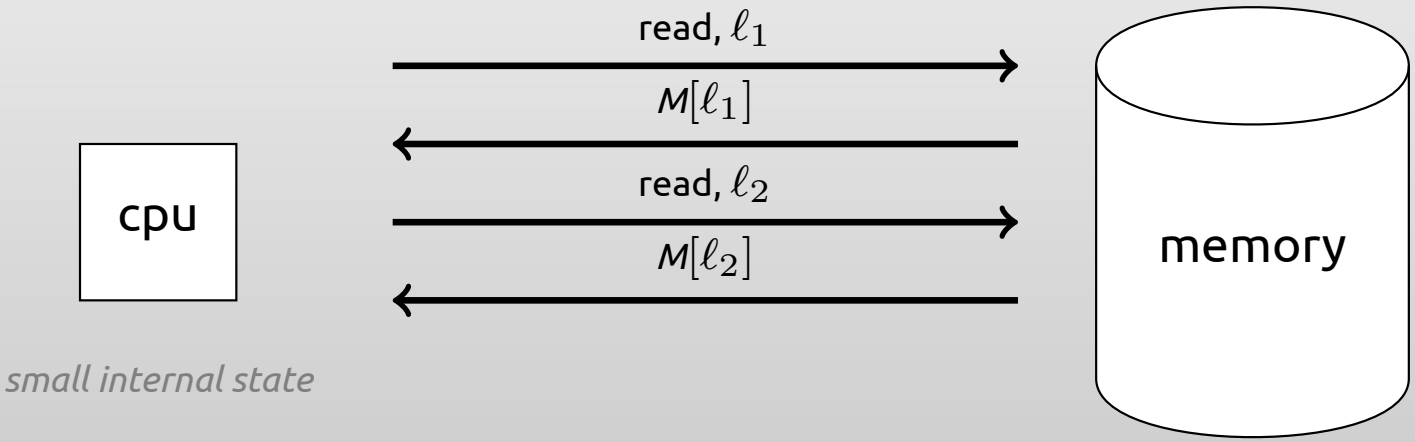

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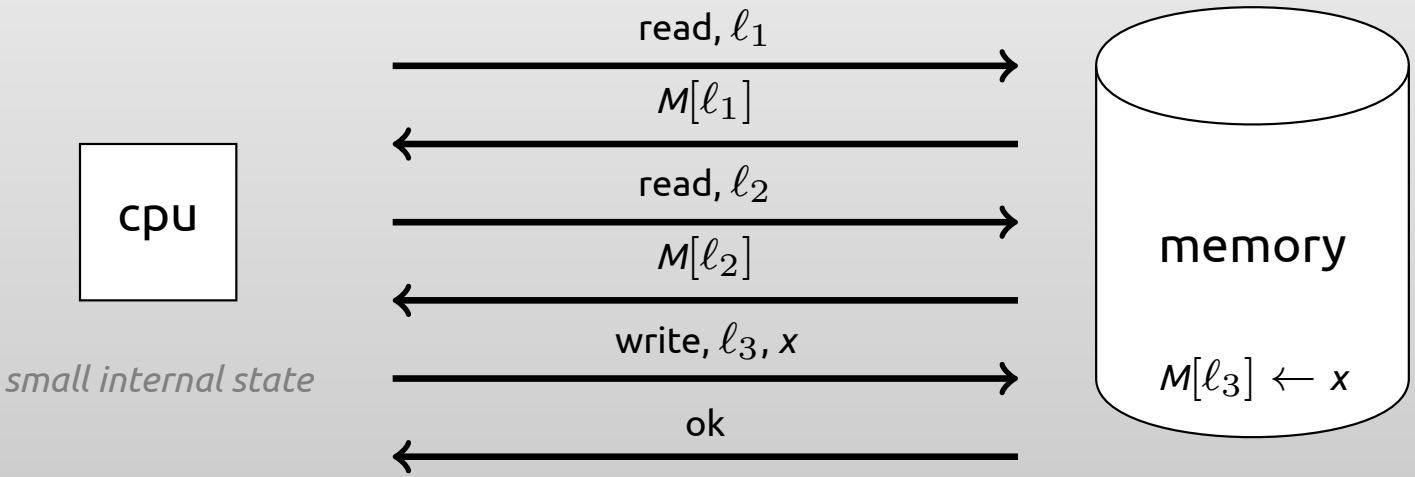

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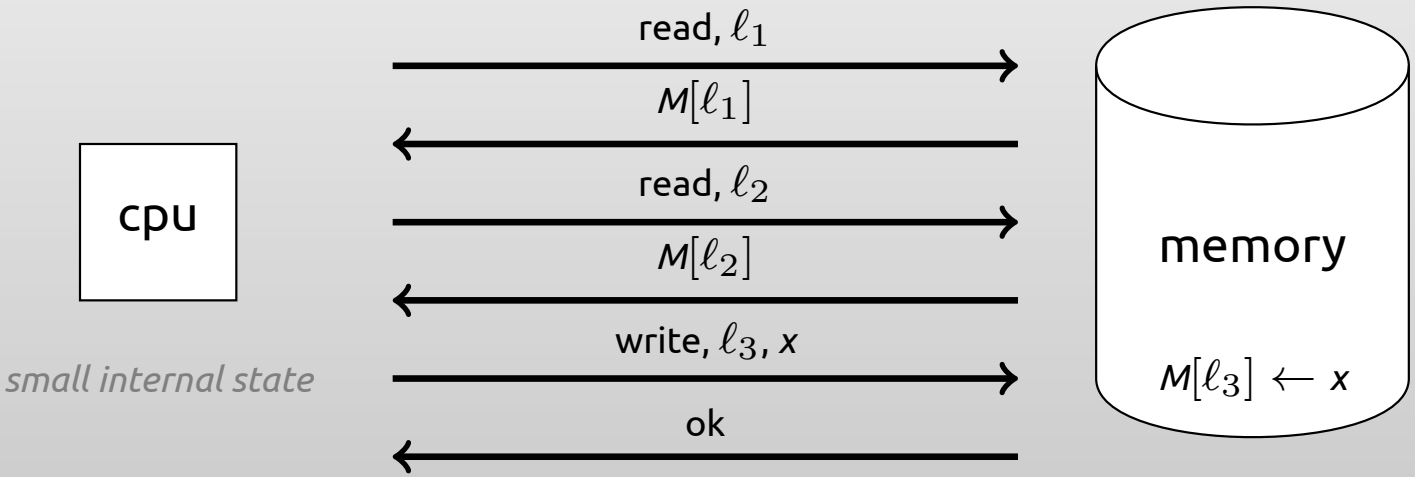
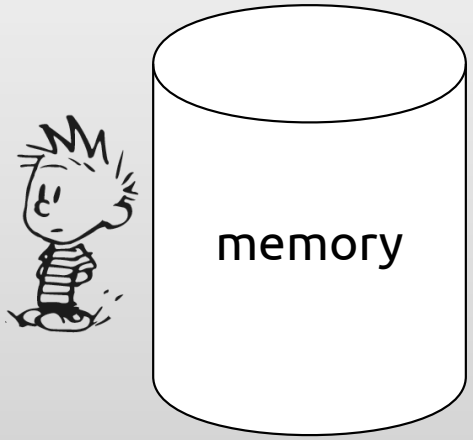


RAM program need not touch every bit of memory.

Idea: securely evaluate RAM



Basic outline:

- Imagine both parties' inputs stored in large memory

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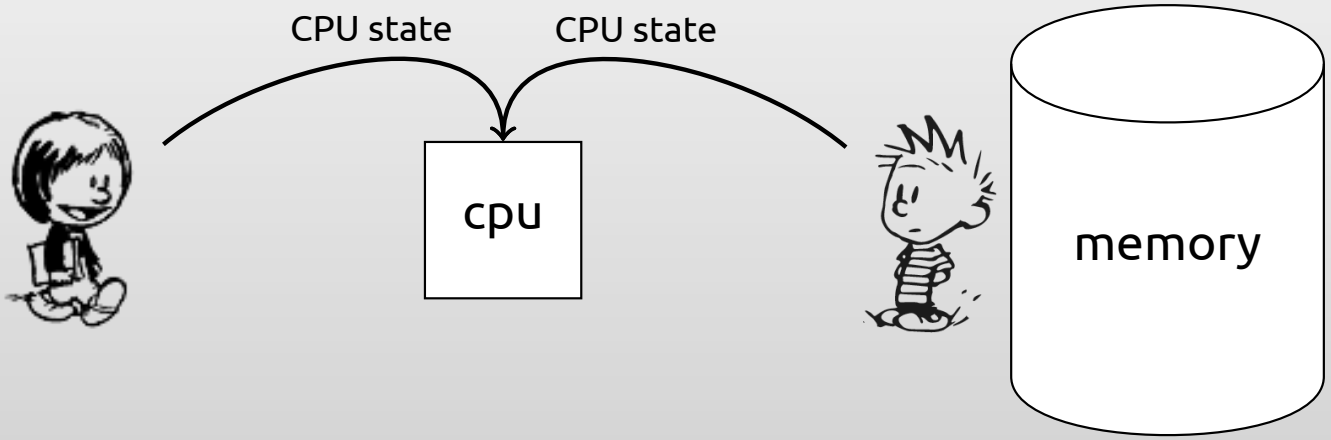

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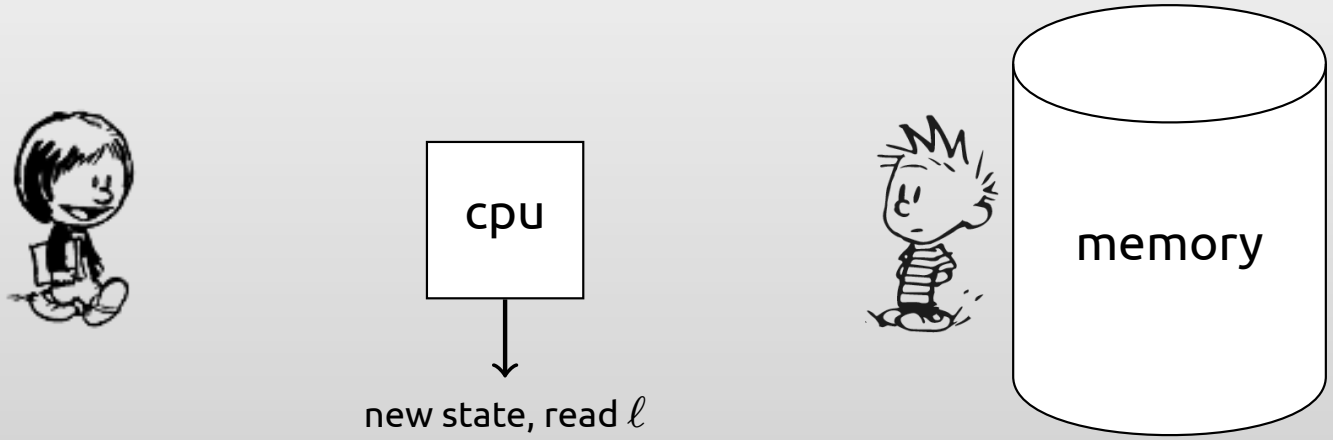

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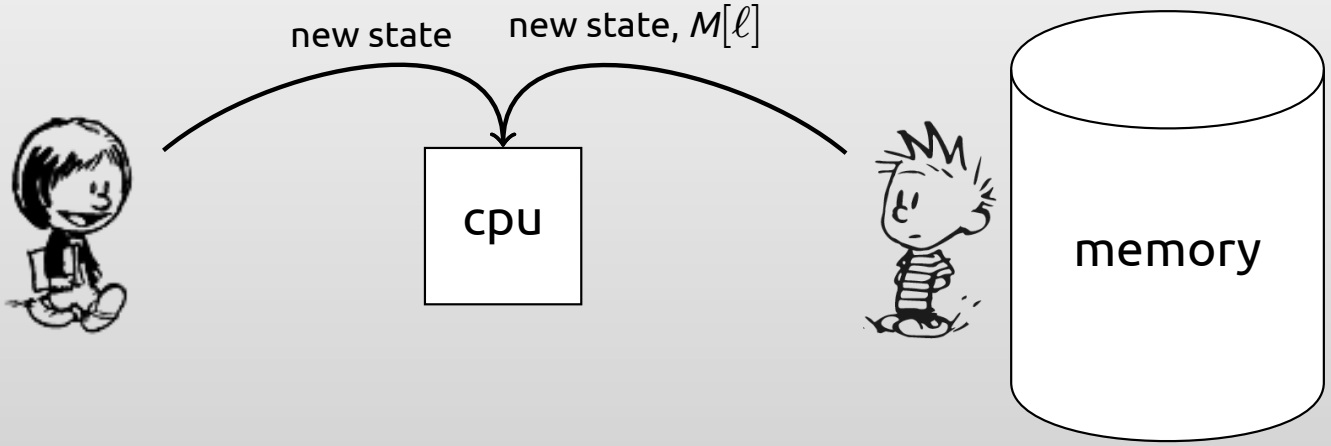

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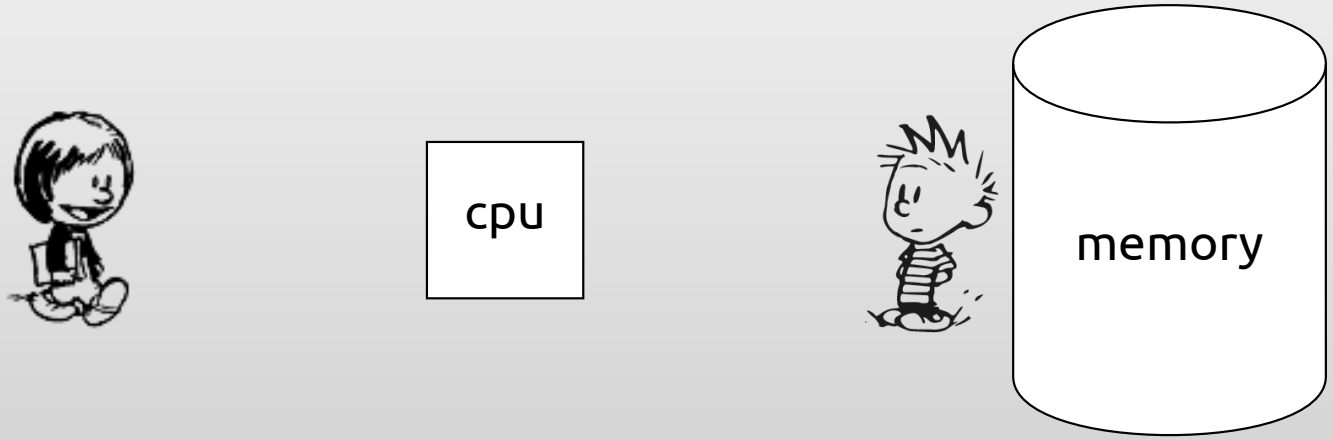

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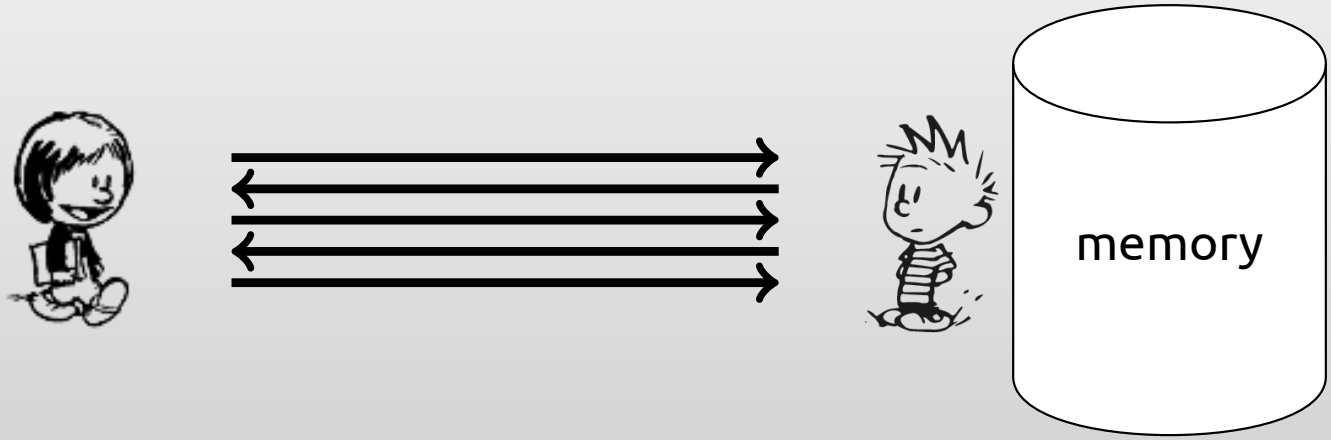

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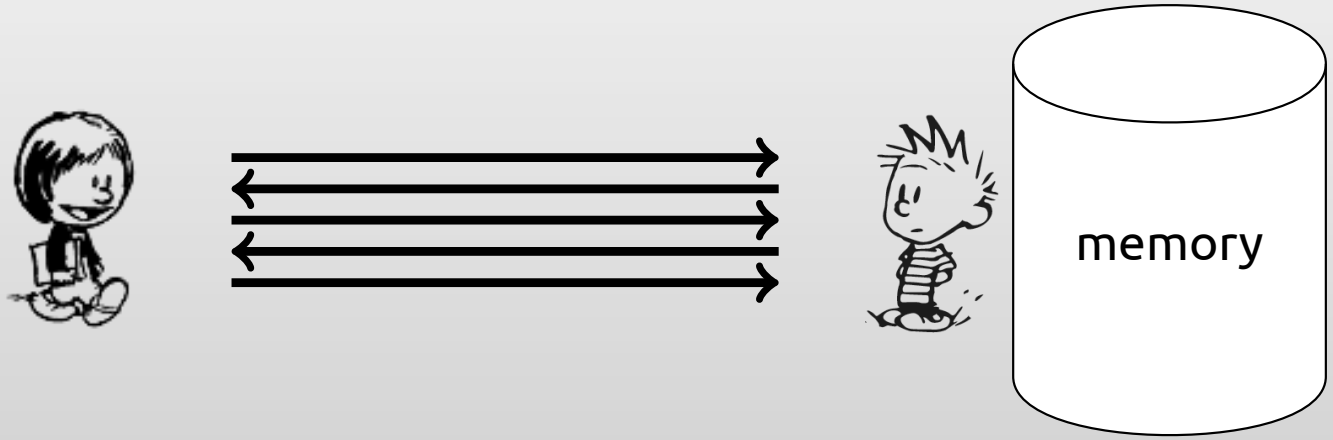

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Cost = (size of next-instruction function) $\times$ (number of instructions)

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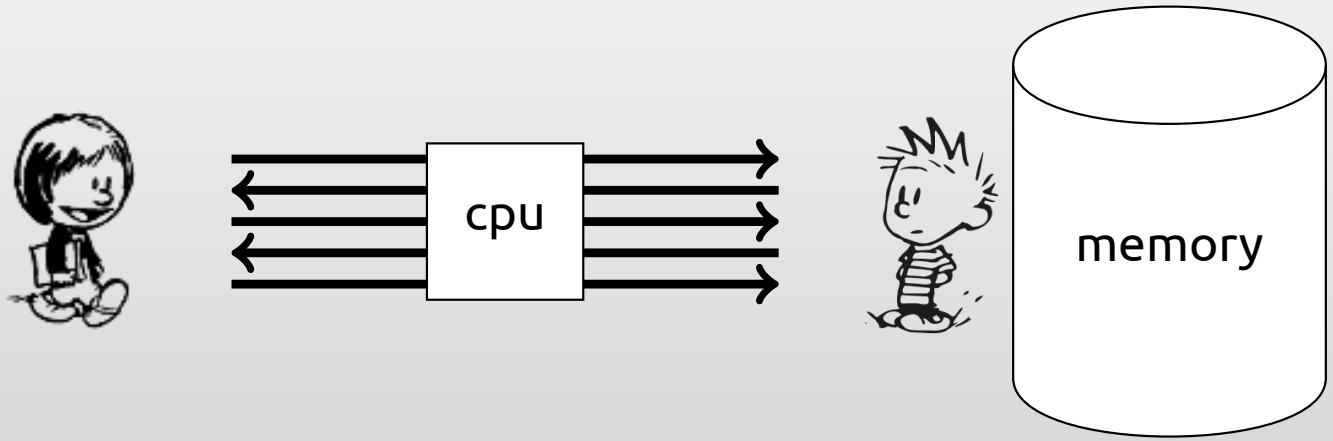

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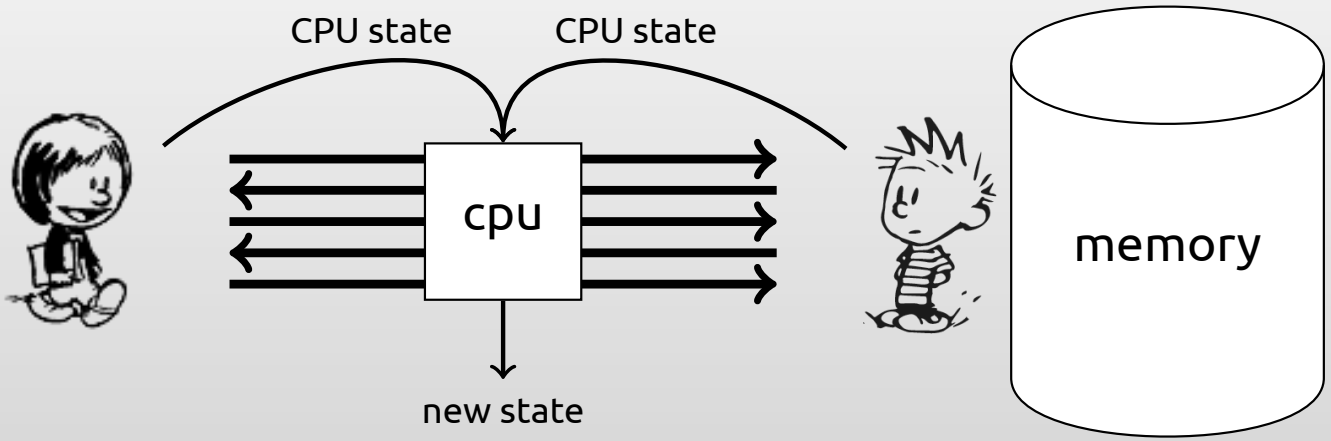

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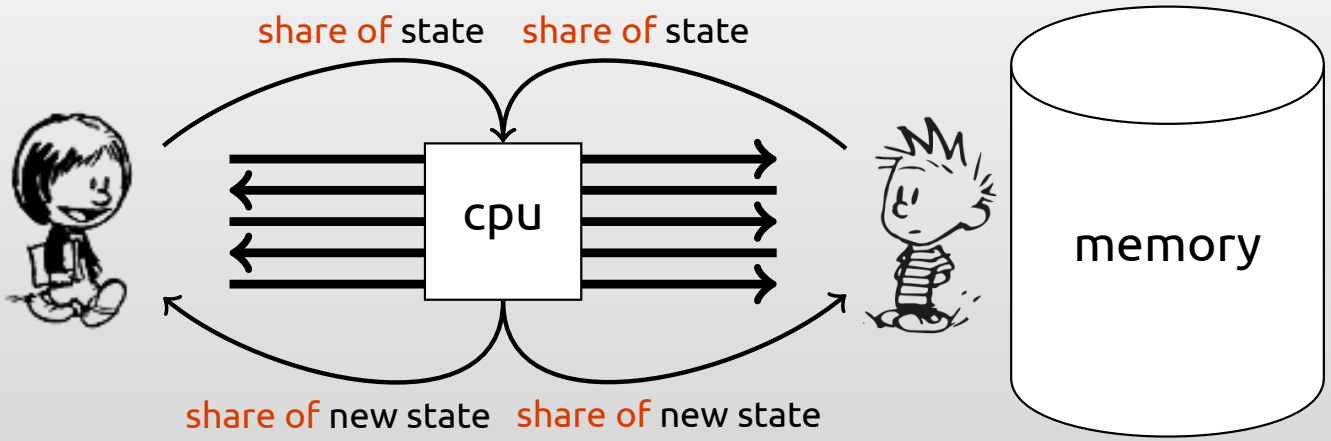

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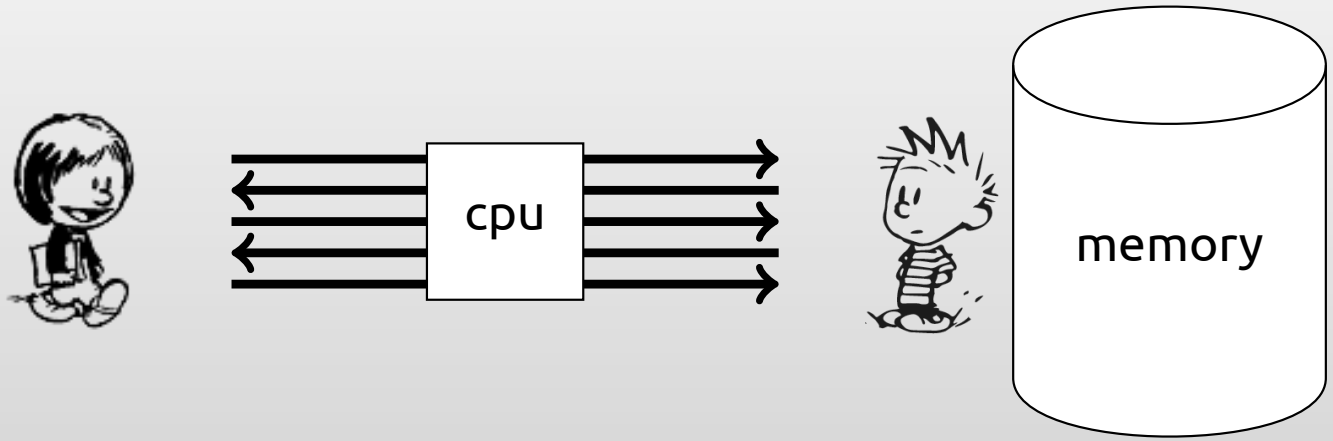

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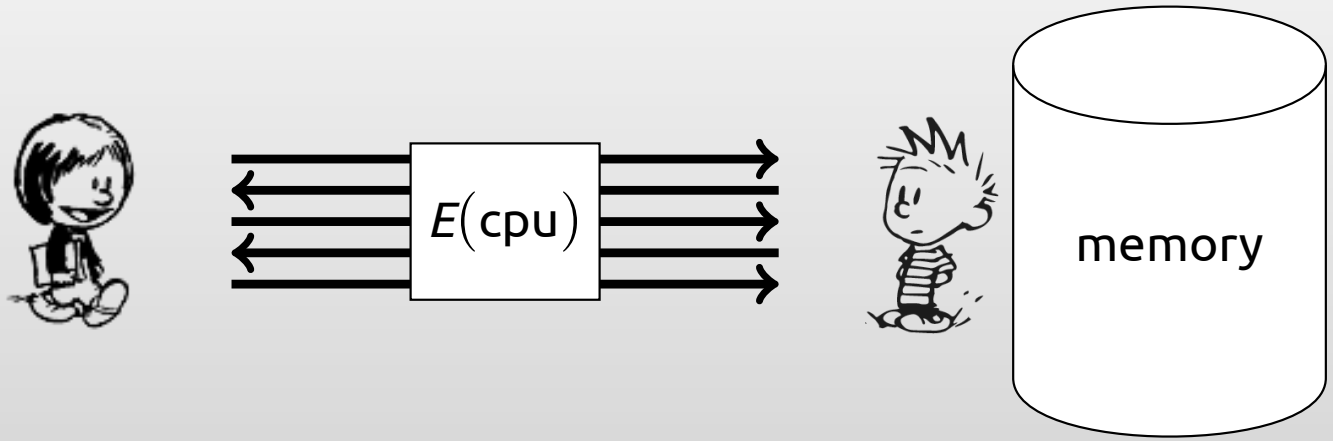

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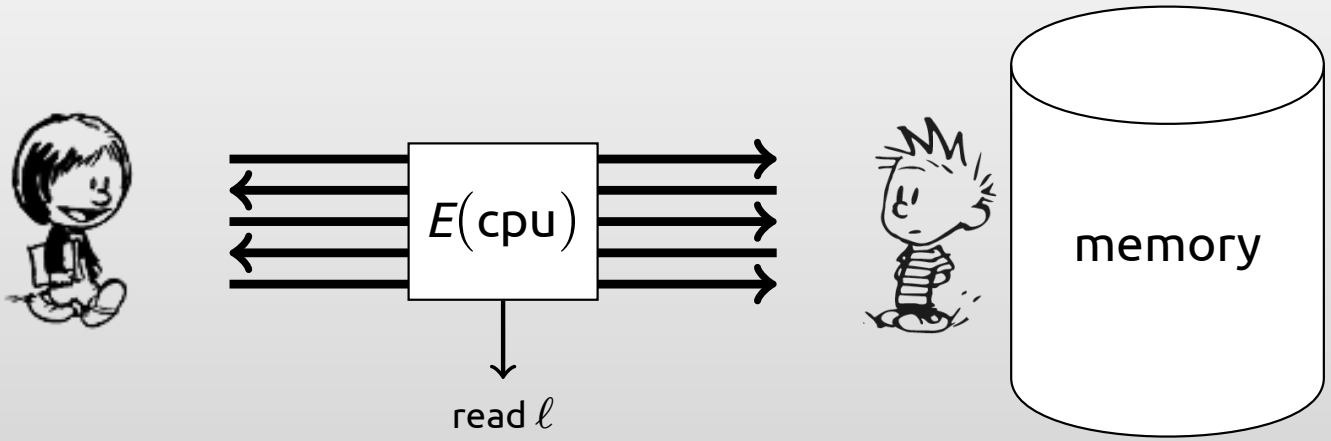

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Memory access pattern (read ℓ_1, write ℓ_2, . . .) public!

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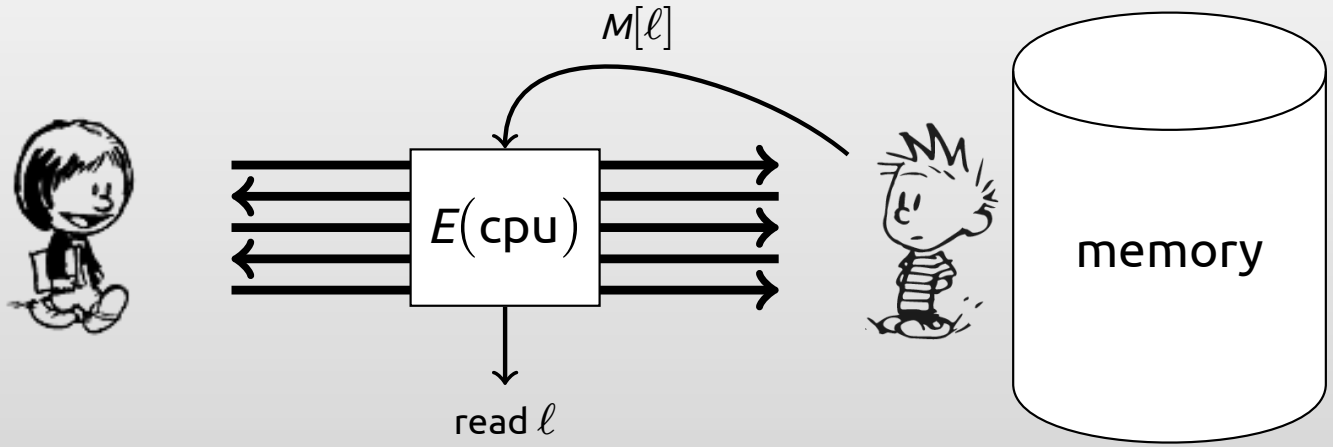

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??? Calvin must learn these so he knows what to do!

Oblivious RAM

Oblivious RAM (ORAM) = memory access pattern leaks nothing about inputs/outputs/state [GoldreichOstrosvky96]

- Can convert any RAM program to ORAM, polylog overhead in runtime & memory [ShiChanStefanovLi11, ...]

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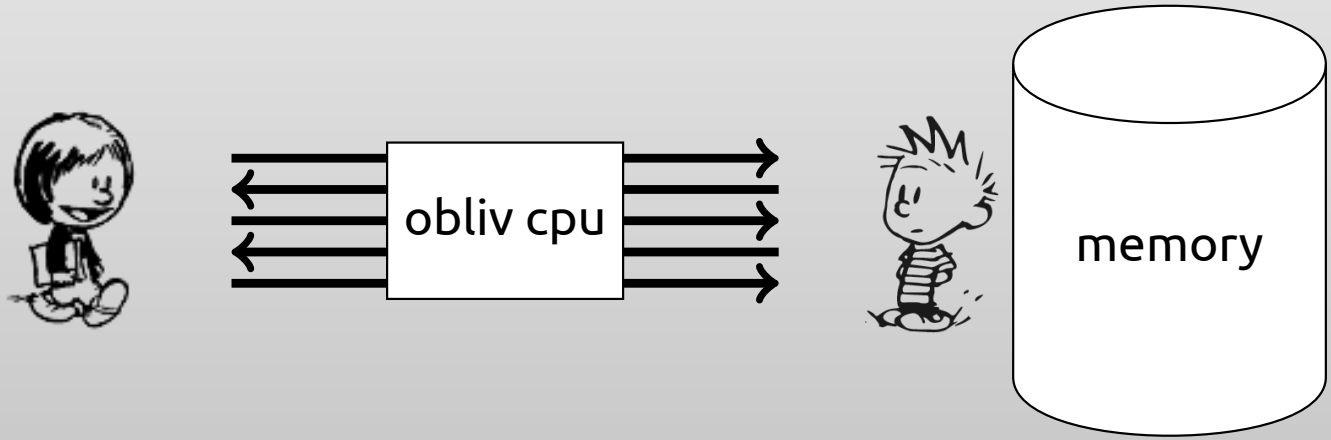

RAM-2PC paradigm [GKKKMRV12]

*"Use traditional 2PC to repeatedly evaluate next-instruction circuit of an **oblivious** RAM program."*

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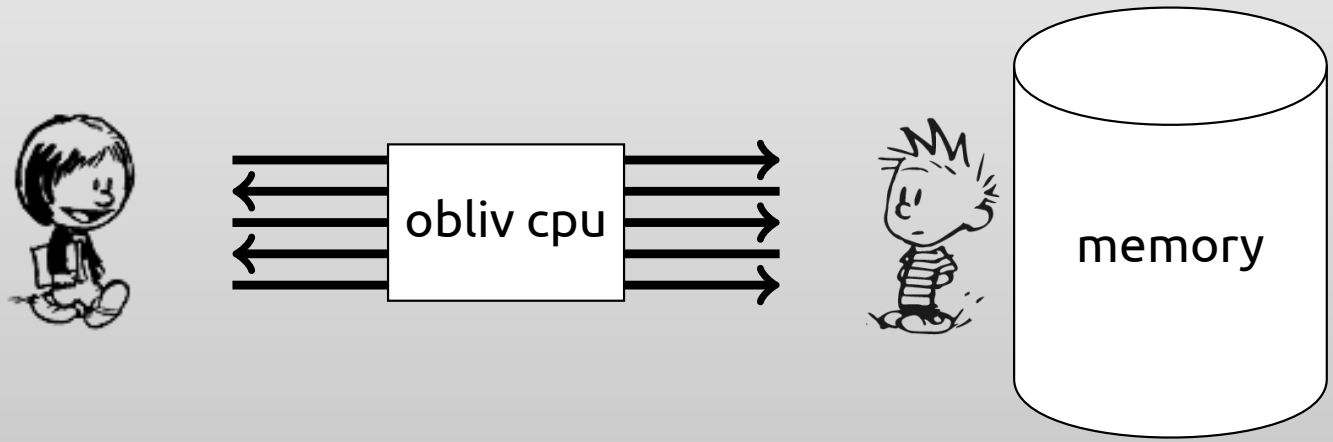

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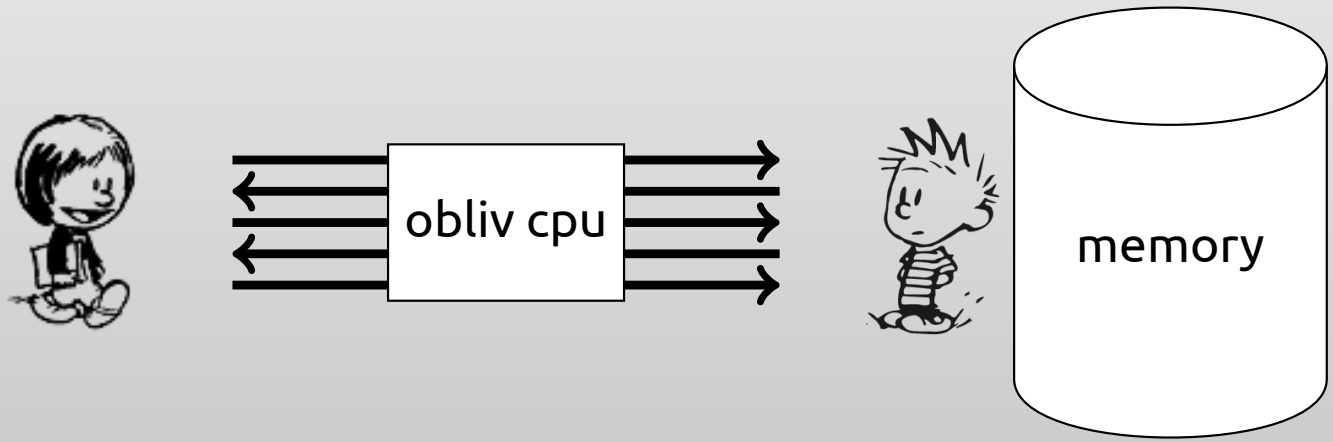

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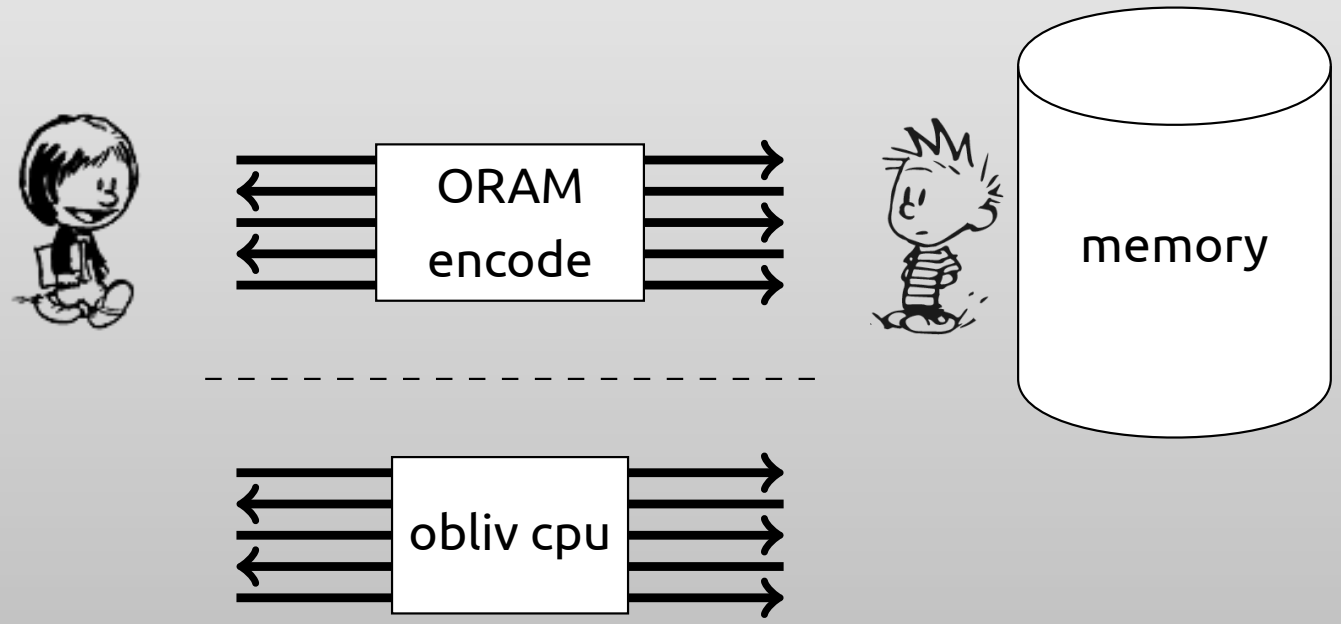

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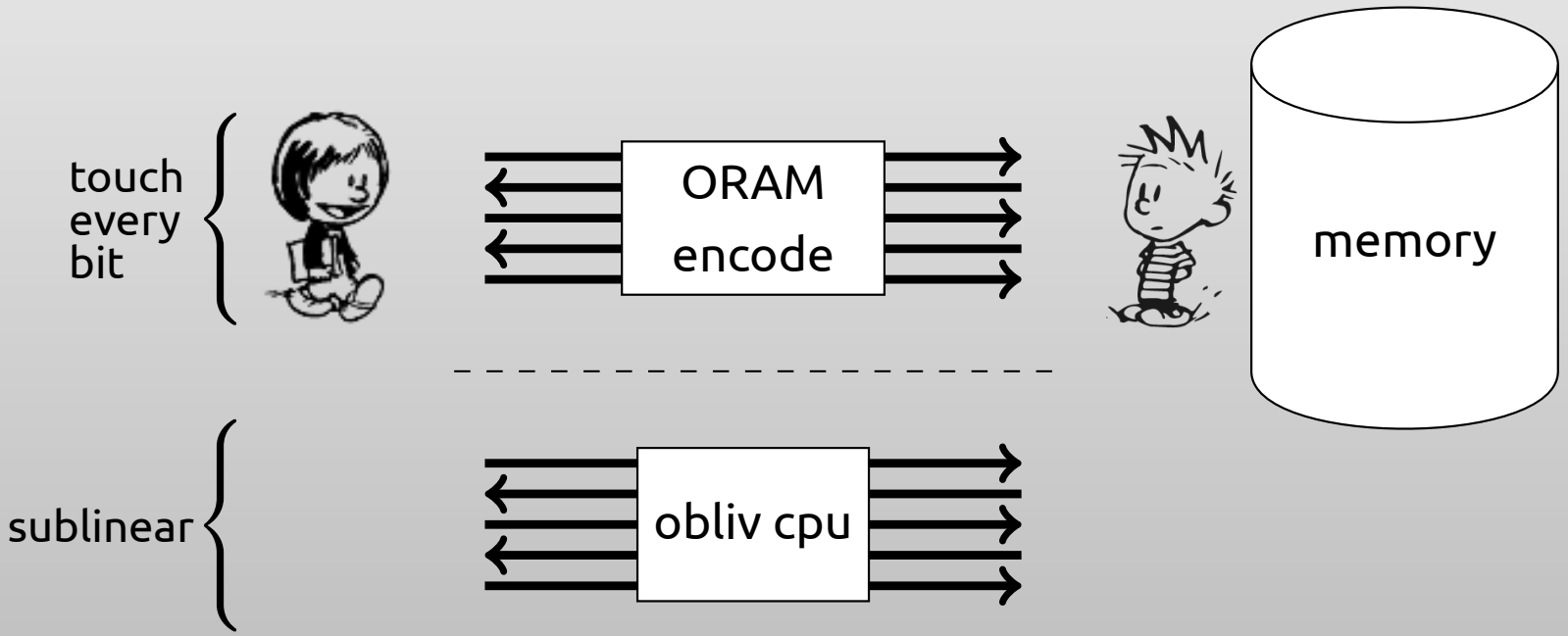
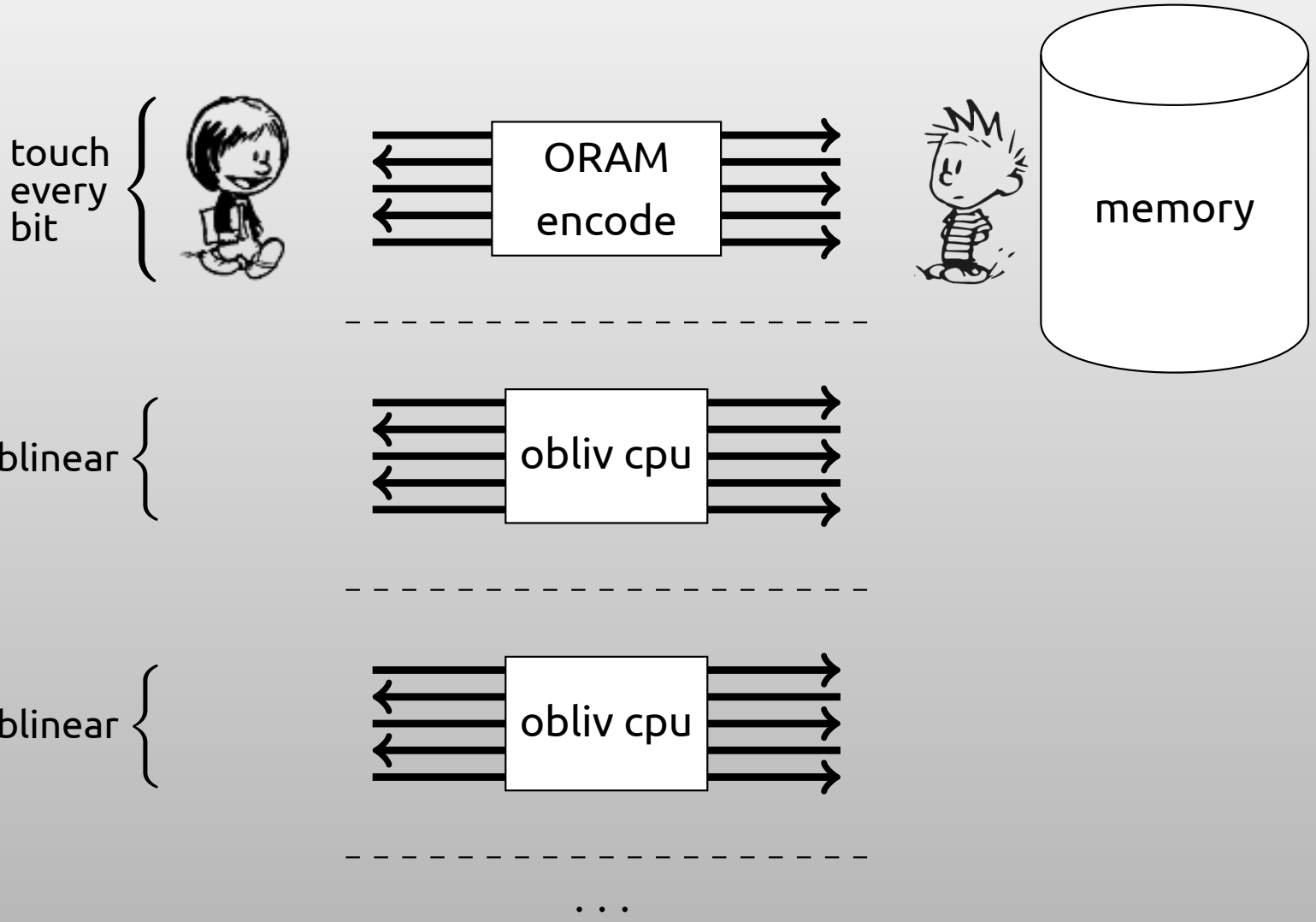


Amortizing

ORAM memory can be reused indefinitely



Summarizing

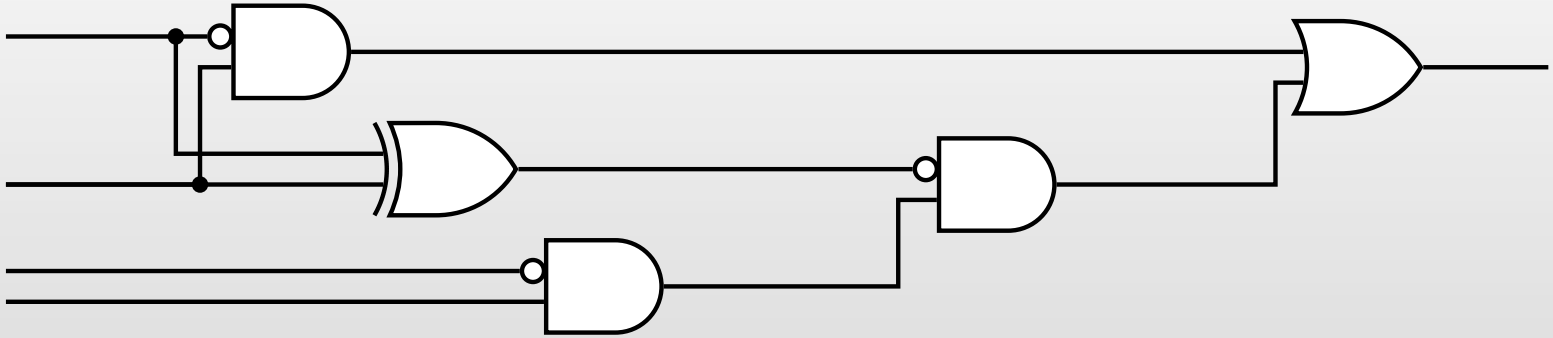
RAM-2PC paradigm [GKKKMRV12]

*"Use traditional 2PC to repeatedly evaluate next-instruction circuit of an **oblivious** RAM program."*

- Expensive $O(N)$ initialization phase
- Subsequent computations cost $\widetilde{O}(T)$, where $T =$ ORAM running time.

- [GKKKMRV12]: semi-honest security
- [AfsharHuMohasselR15]: malicious security
- [HuMohasselR15]: malicious security, one-sided privacy

Garbled circuit framework [Yao86]



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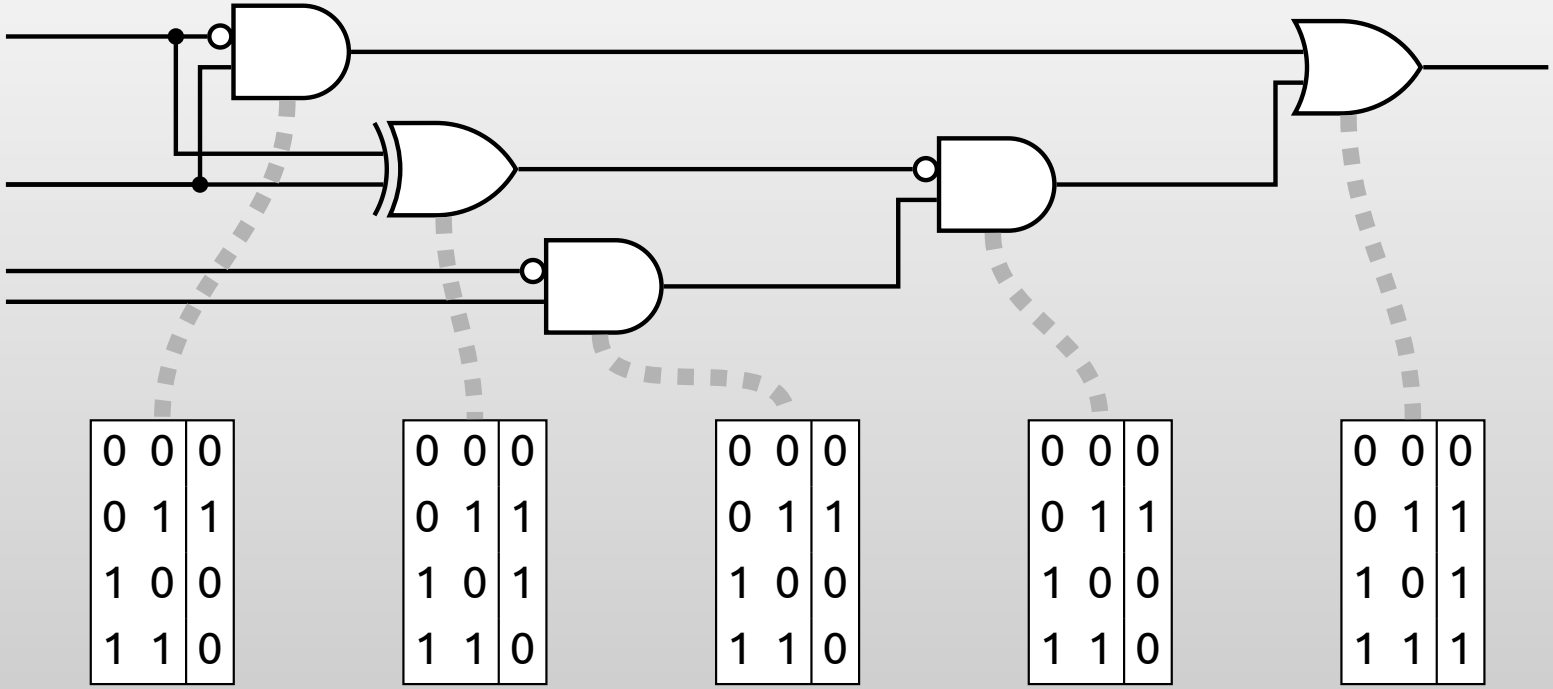

0	0	0
0	1	1
1	0	0
1	1	0

0	0	0
0	1	1
1	0	1
1	1	0

0	0	0
0	1	1
1	0	0
1	1	0

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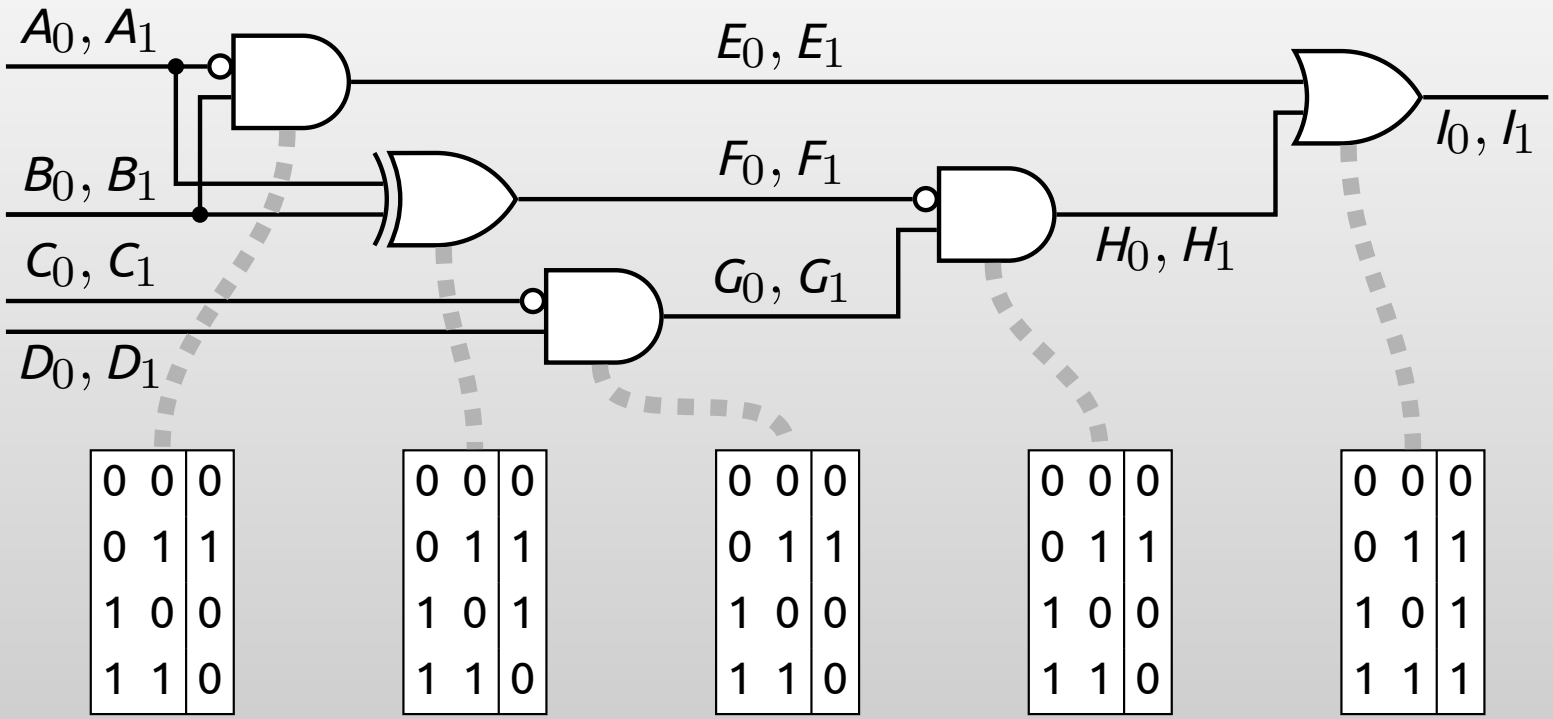

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- Pick random **labels** W_0, W_1 on each wire

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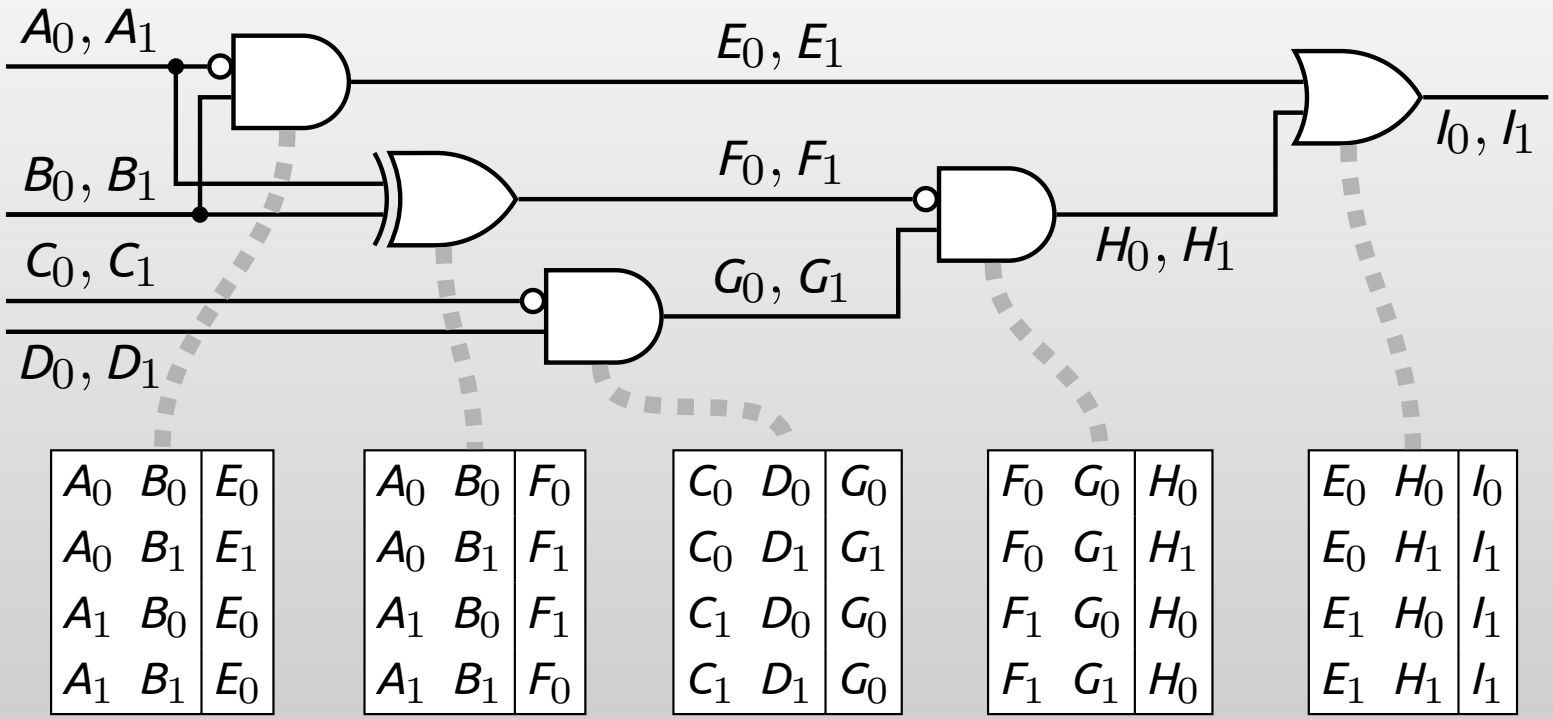

A_0	B_0	E_0
A_0	B_1	E_1
A_1	B_0	E_0
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A_0	B_0	F_0
A_0	B_1	F_1
A_1	B_0	F_1
A_1	B_1	F_0

C_0	D_0	G_0
C_0	D_1	G_1
C_1	D_0	G_0
C_1	D_1	G_0

F_0	G_0	H_0
F_0	G_1	H_1
F_1	G_0	H_0
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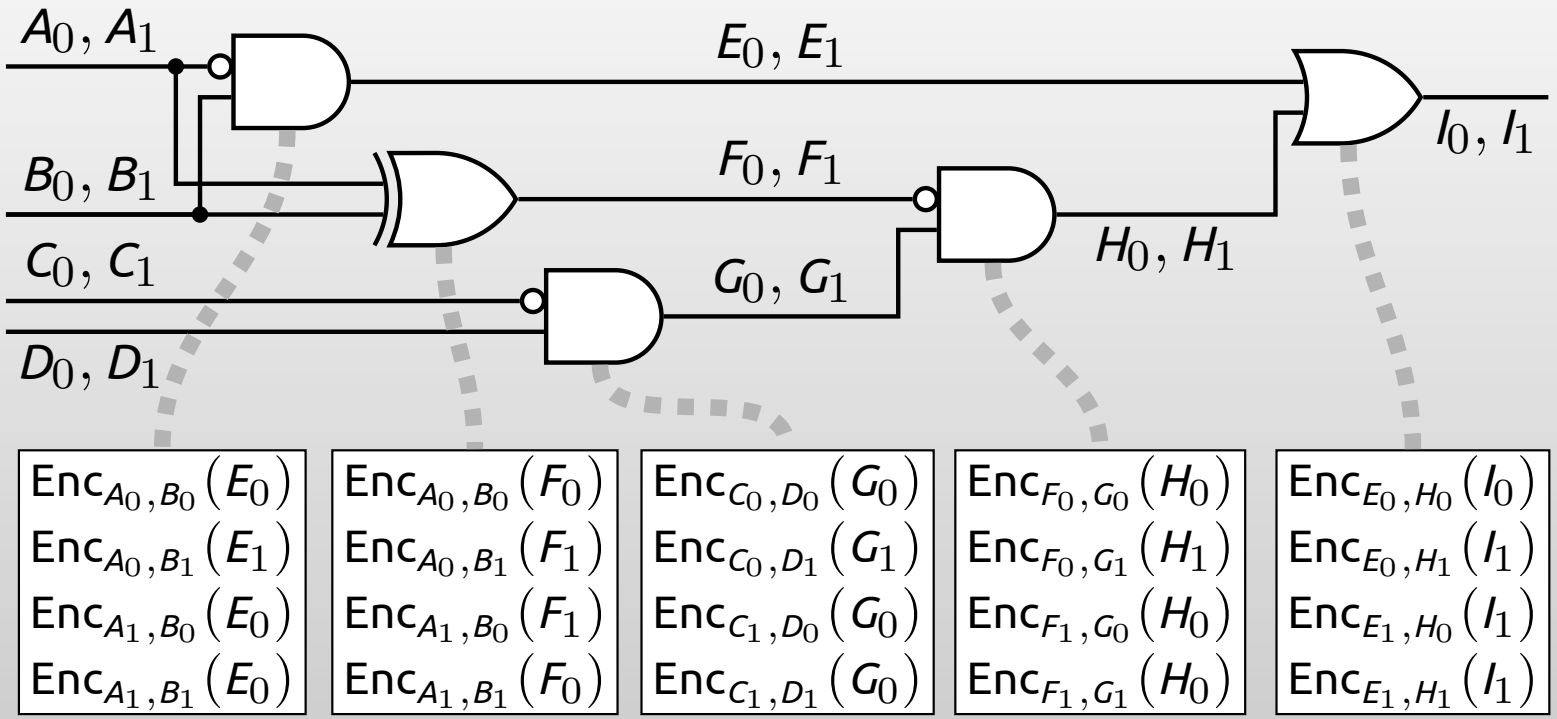

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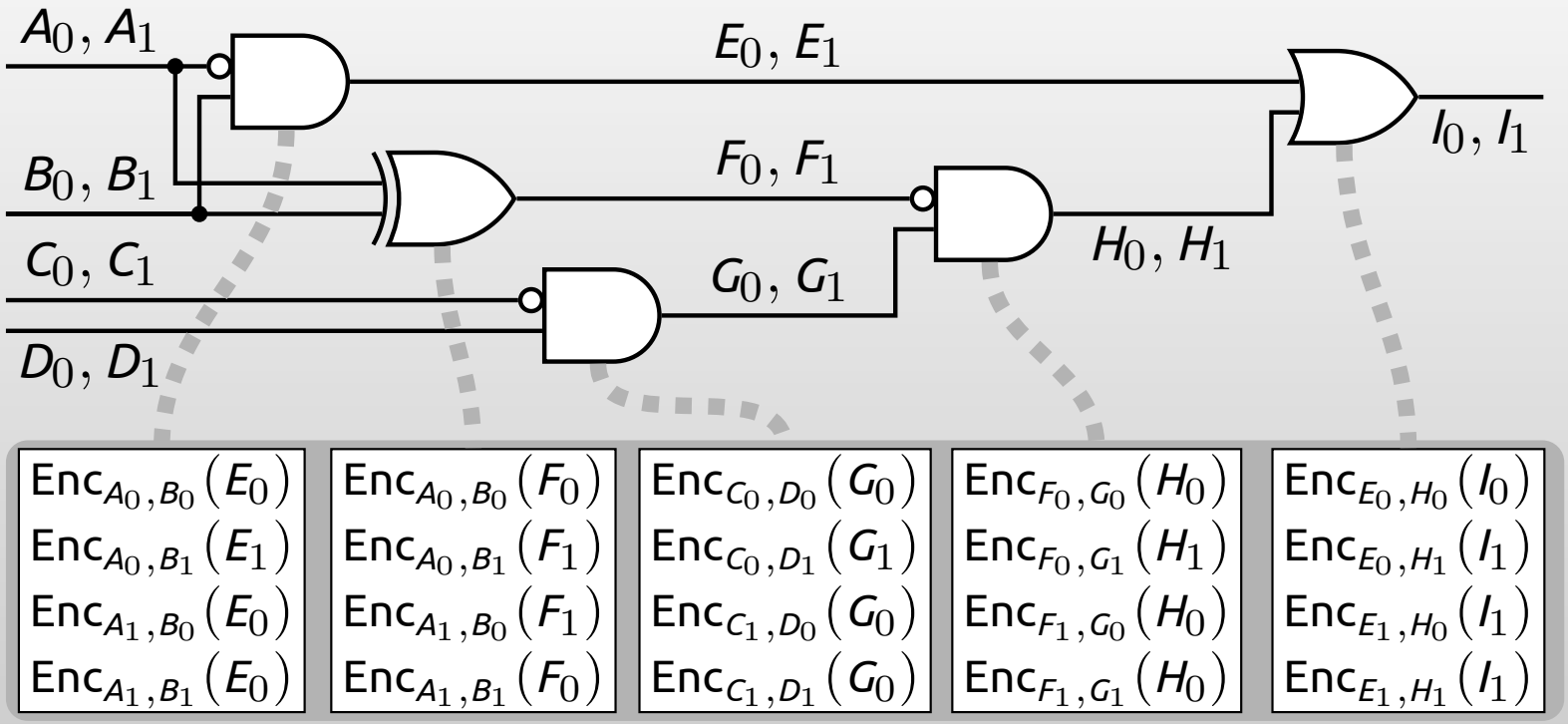

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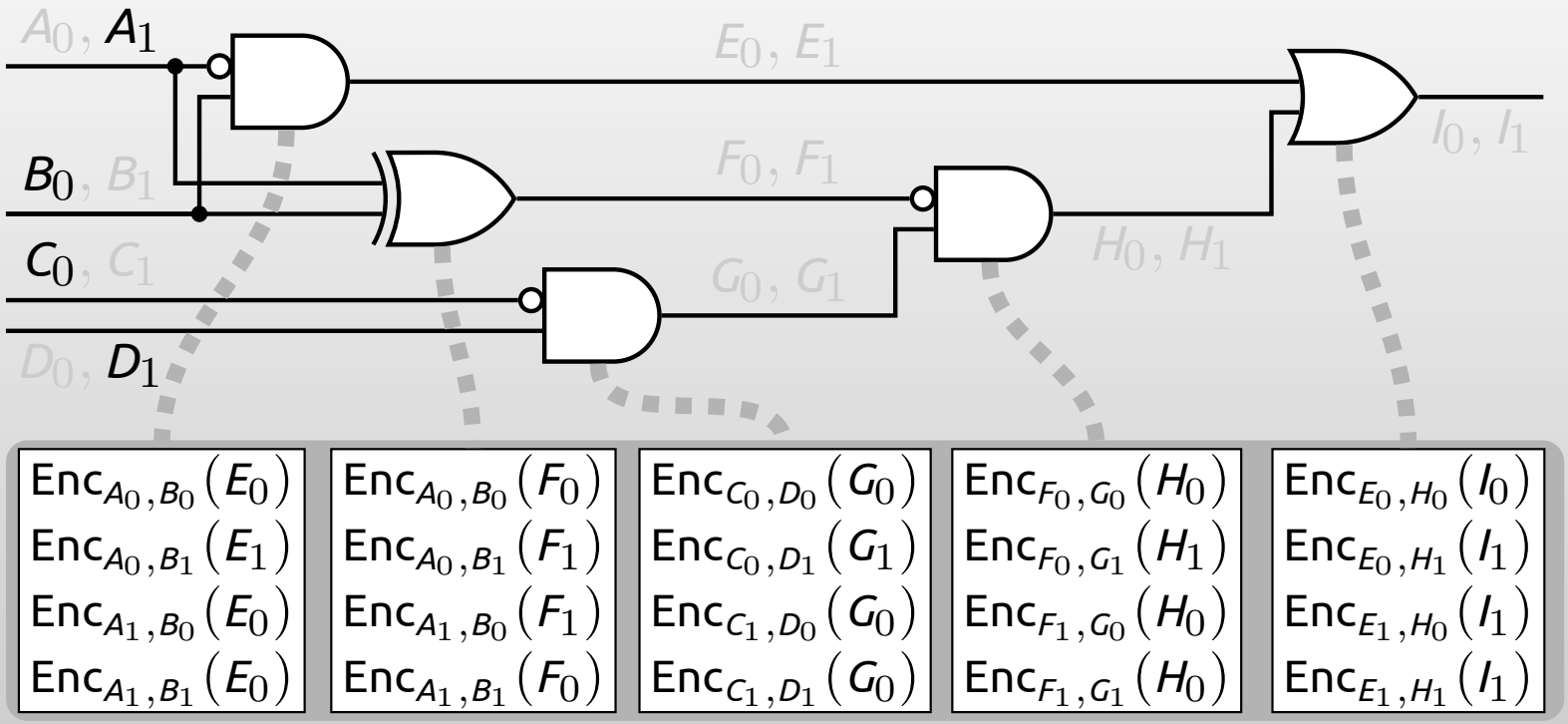

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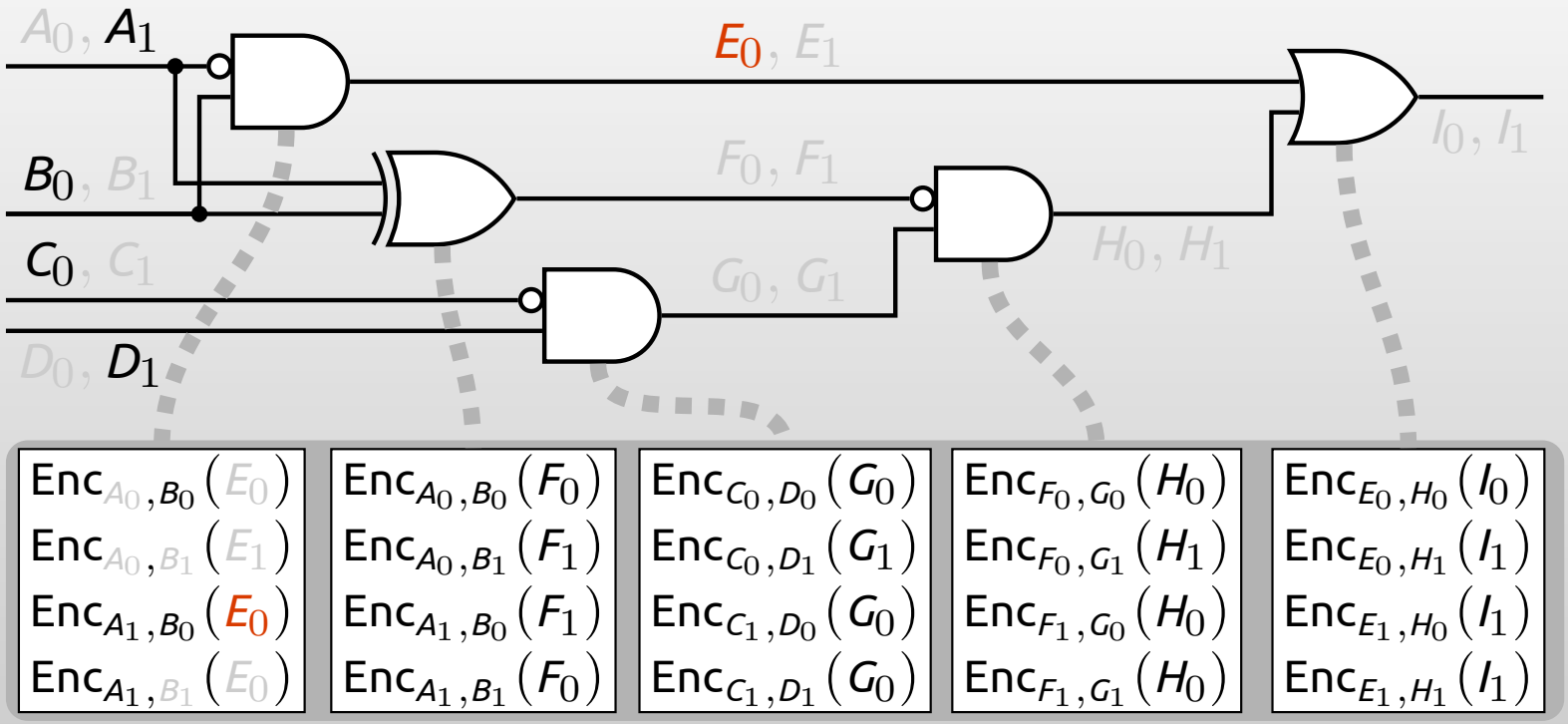

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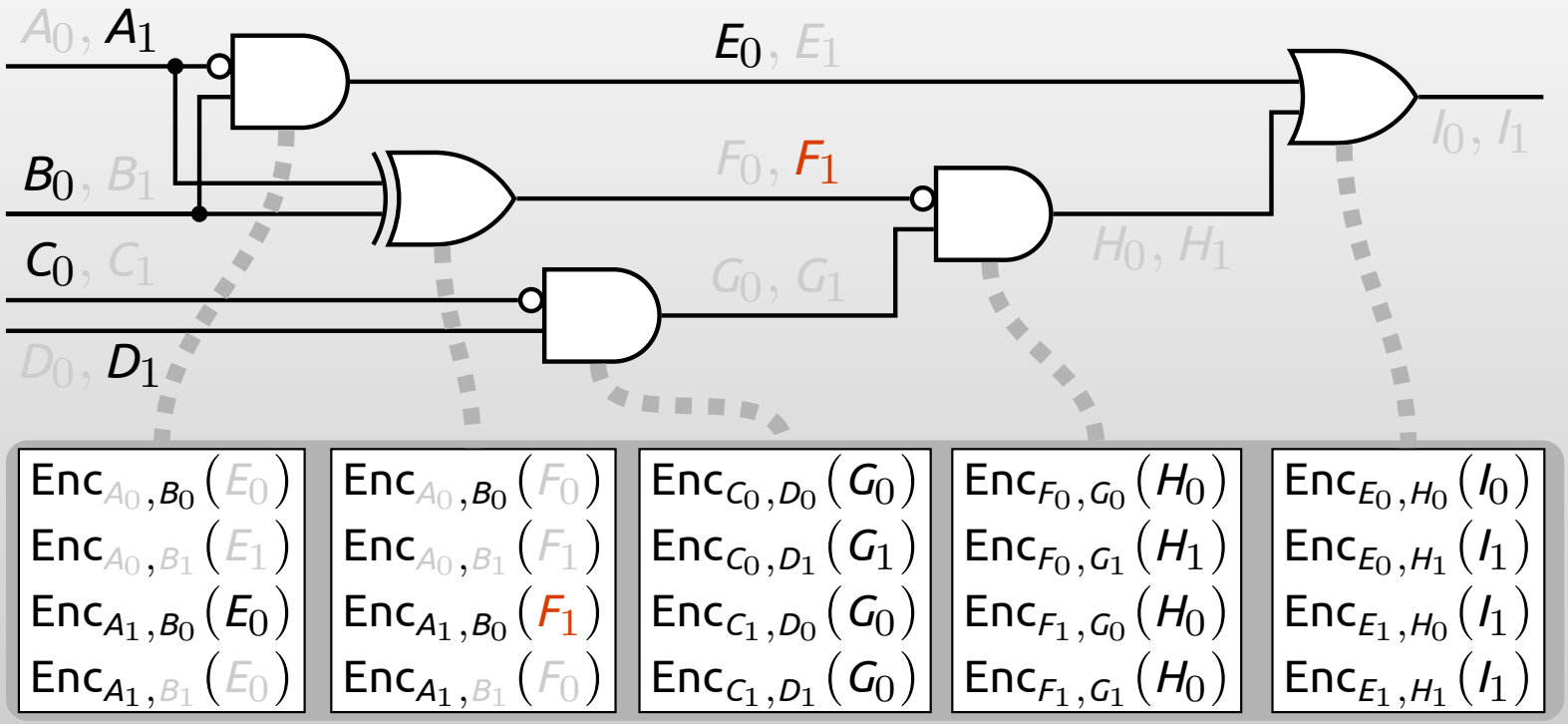

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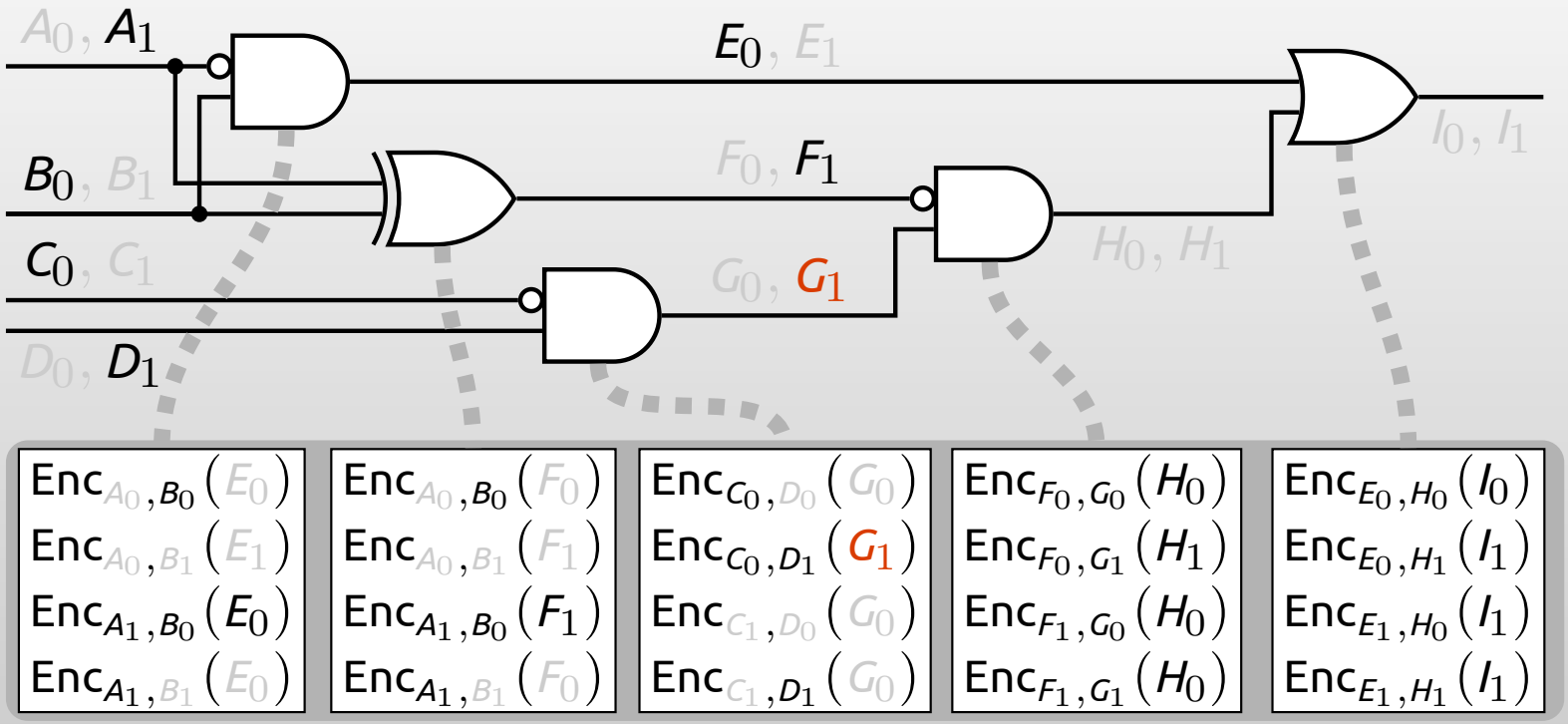

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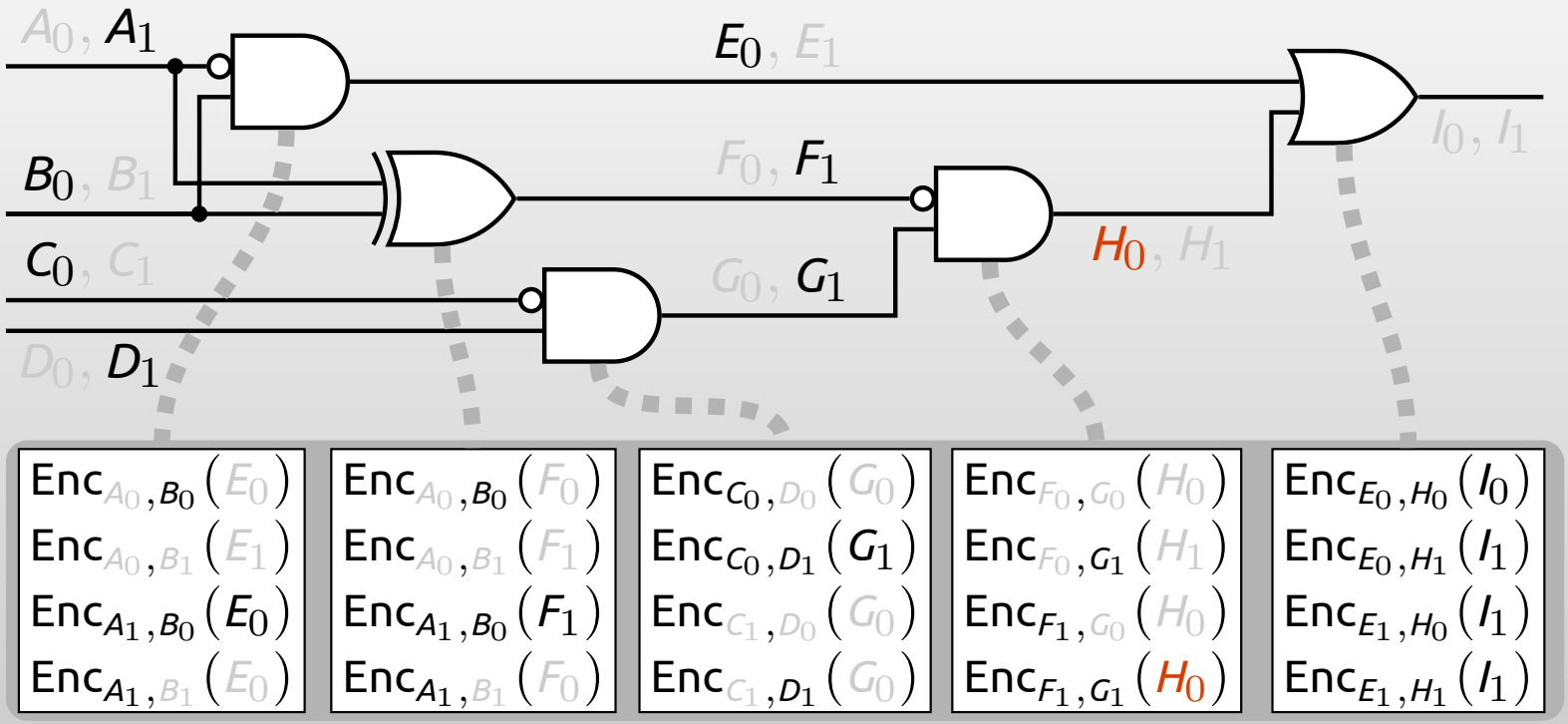
- Only one ciphertext per gate is decryptable
- Result of decryption = value on outgoing wire

Garbled circuit framework [Yao86]



Garbling a circuit:

- Pick random **labels** W_0, W_1 on each wire
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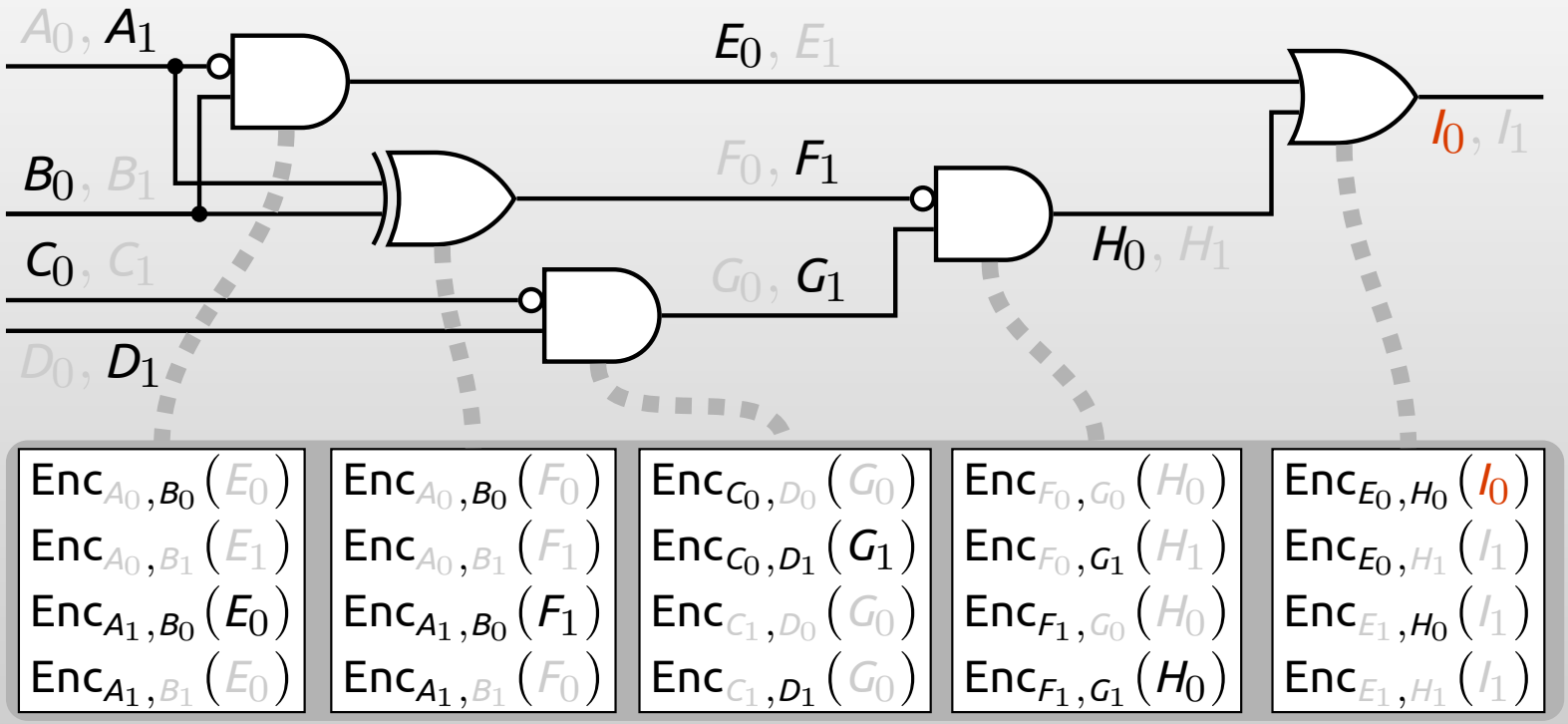

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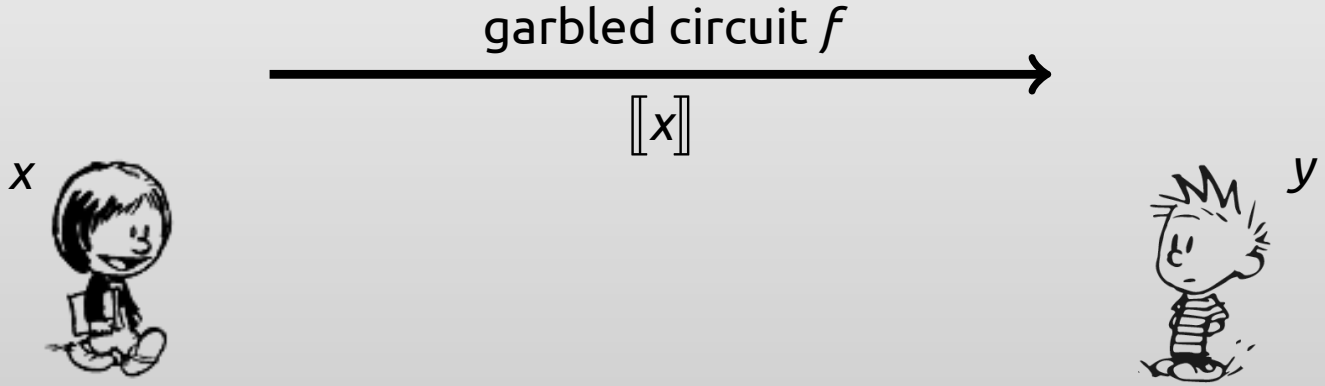

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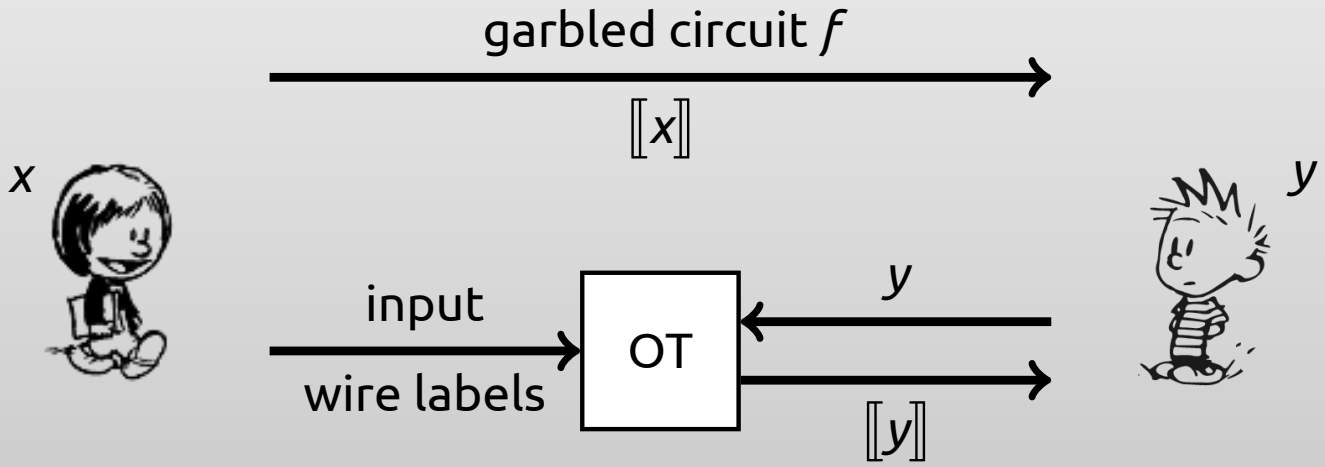

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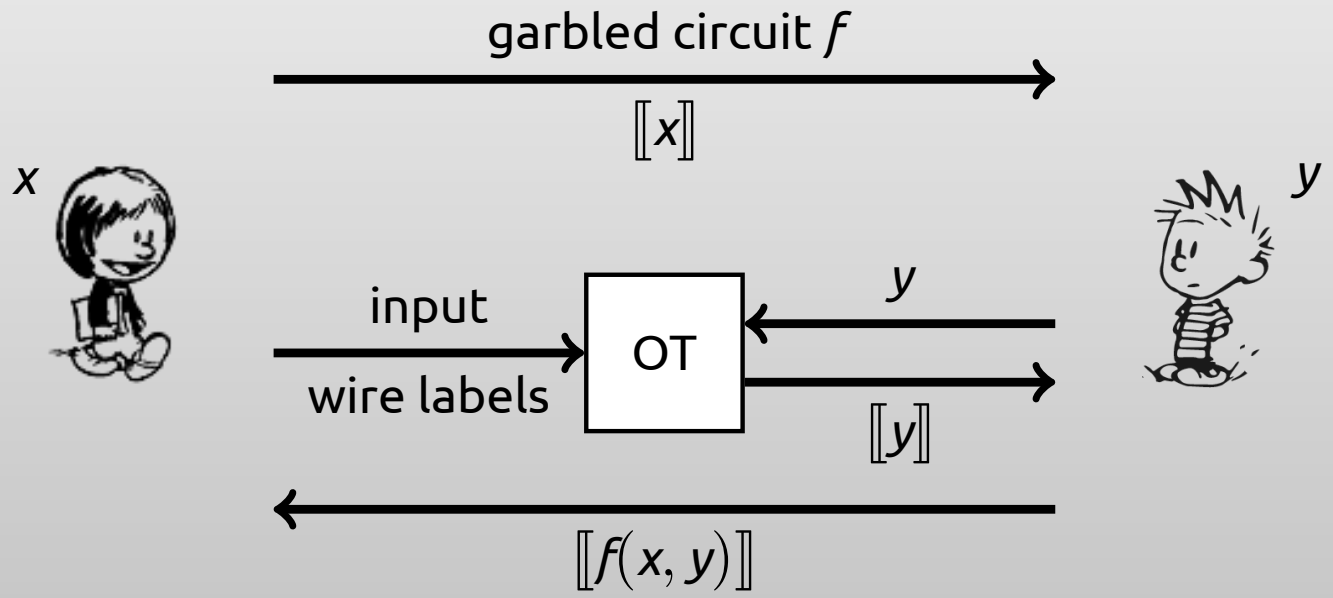

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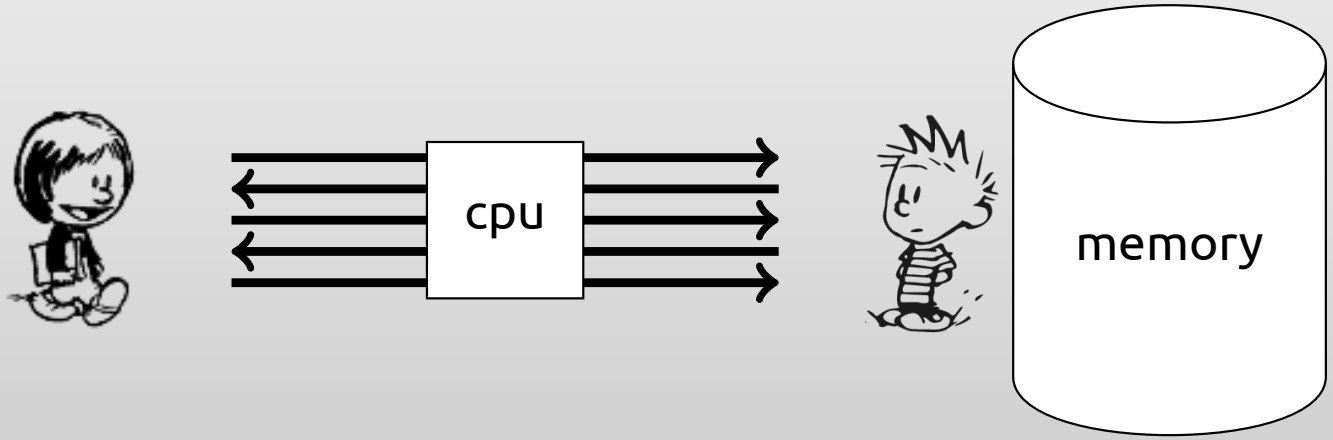

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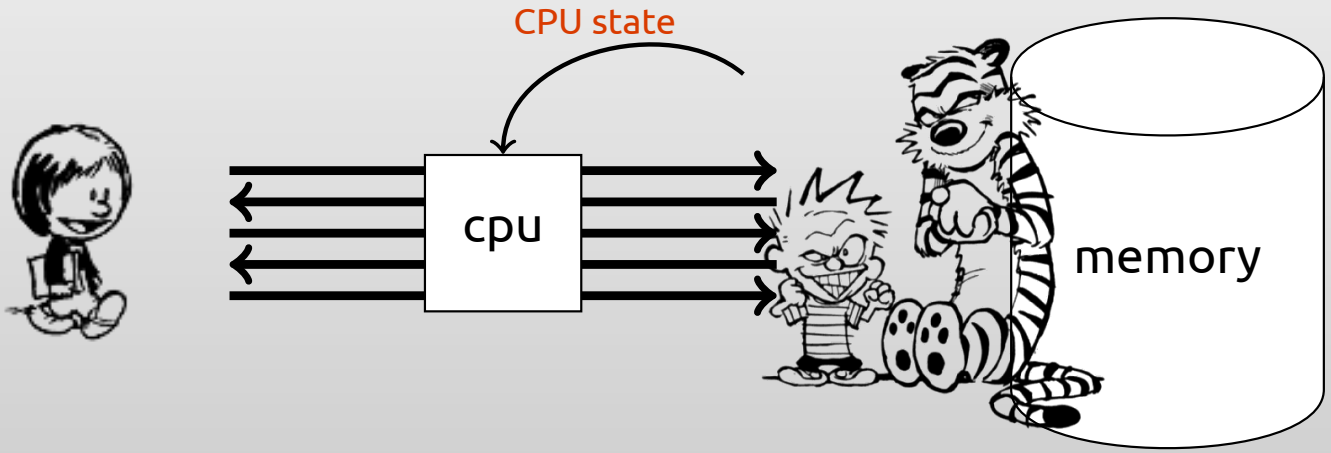

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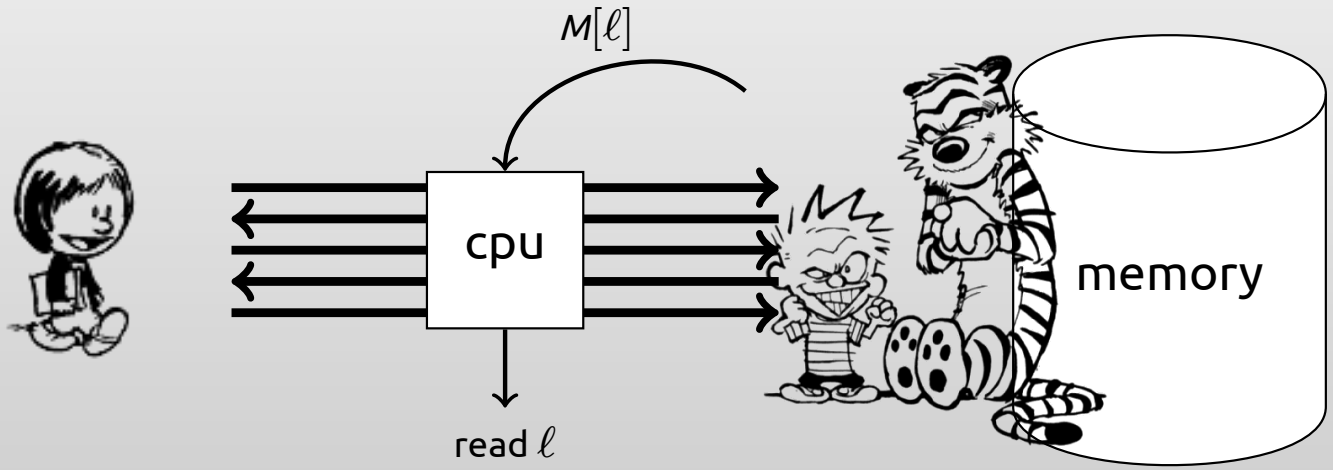

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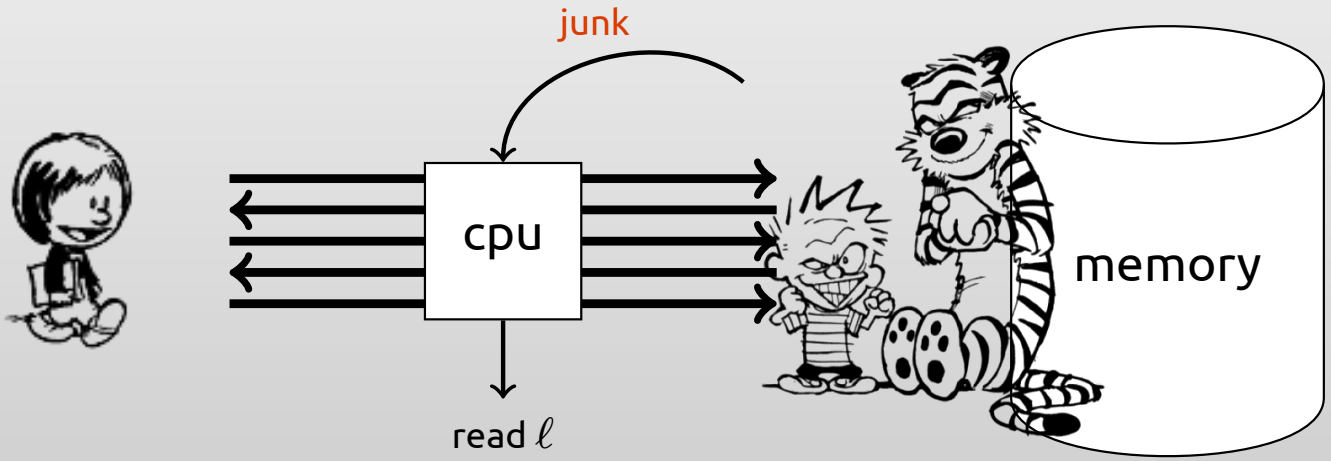

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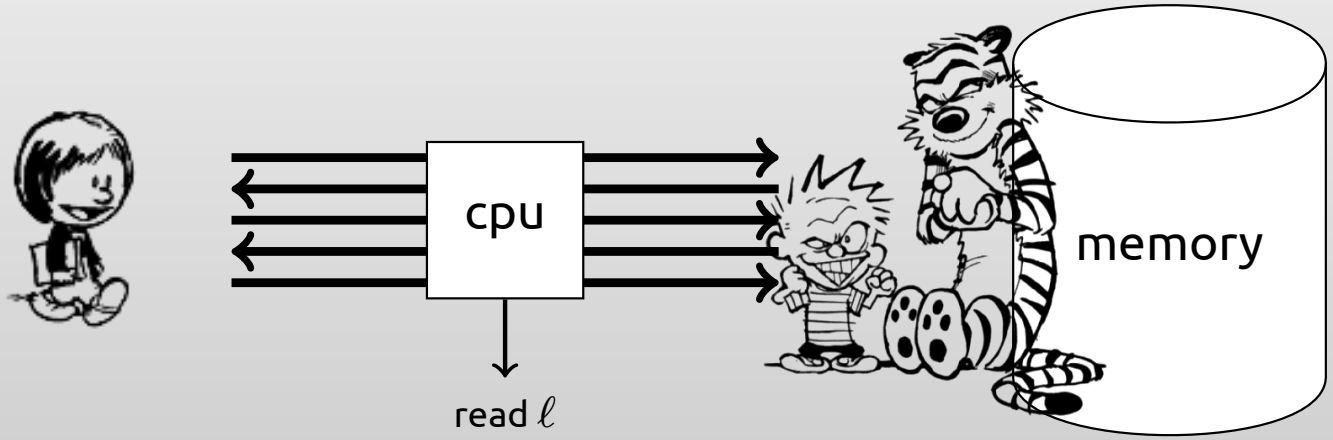

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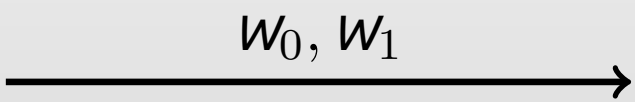
Our approach [AfsharHuMohasselR15]

Idea: represent state/memory [re]using **garbled encodings!**



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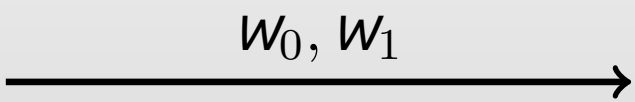

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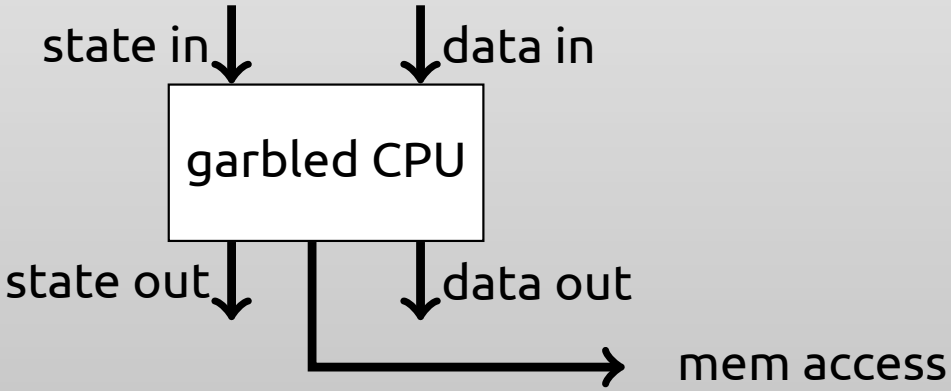
Benefits:

- CPU next-instruction circuit doesn't need to encrypt/decrypt (garbled encoding already hides the information)
- CPU next-instruction circuit doesn' need to secret-share CPU state

Reusing garbled encodings



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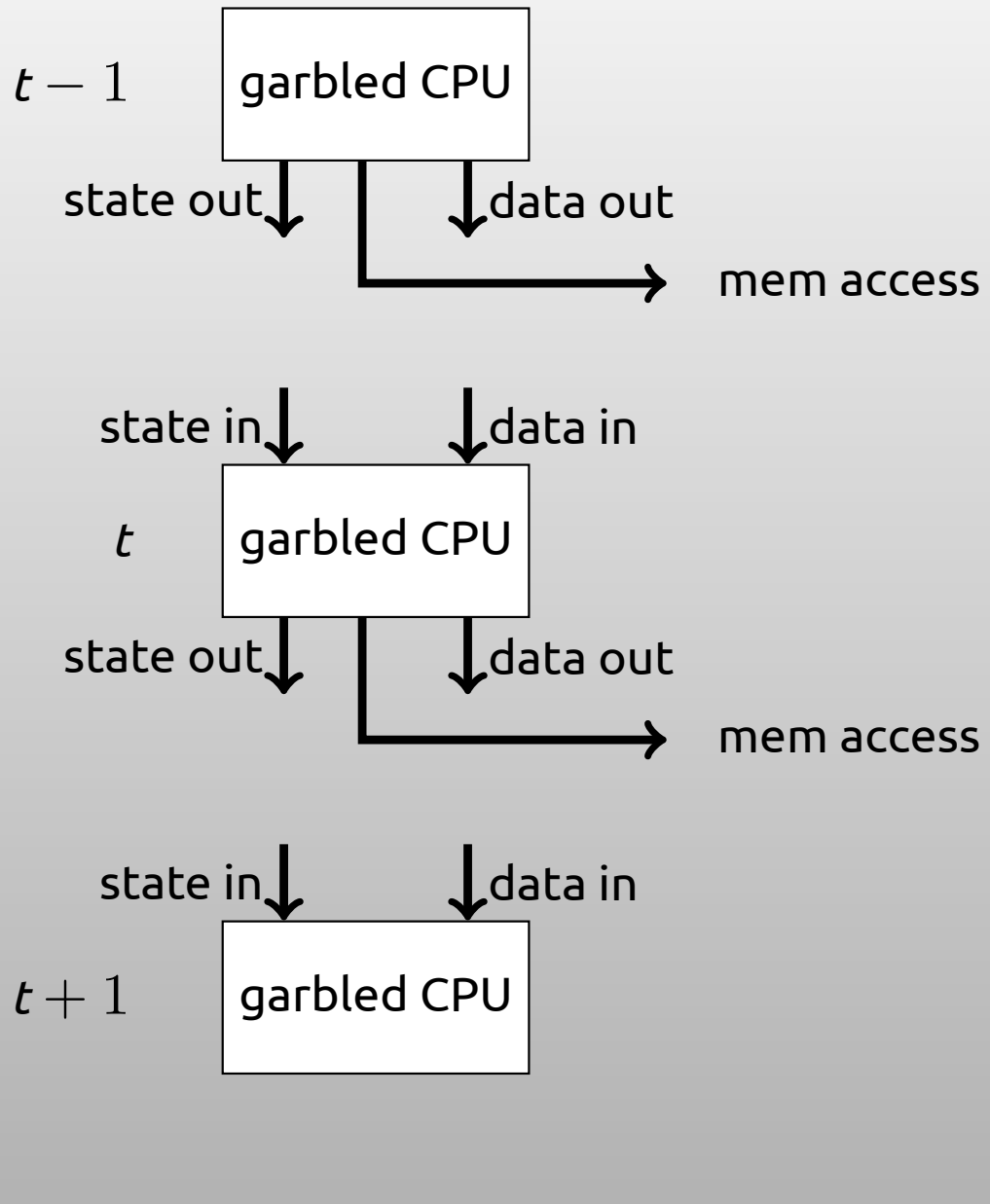

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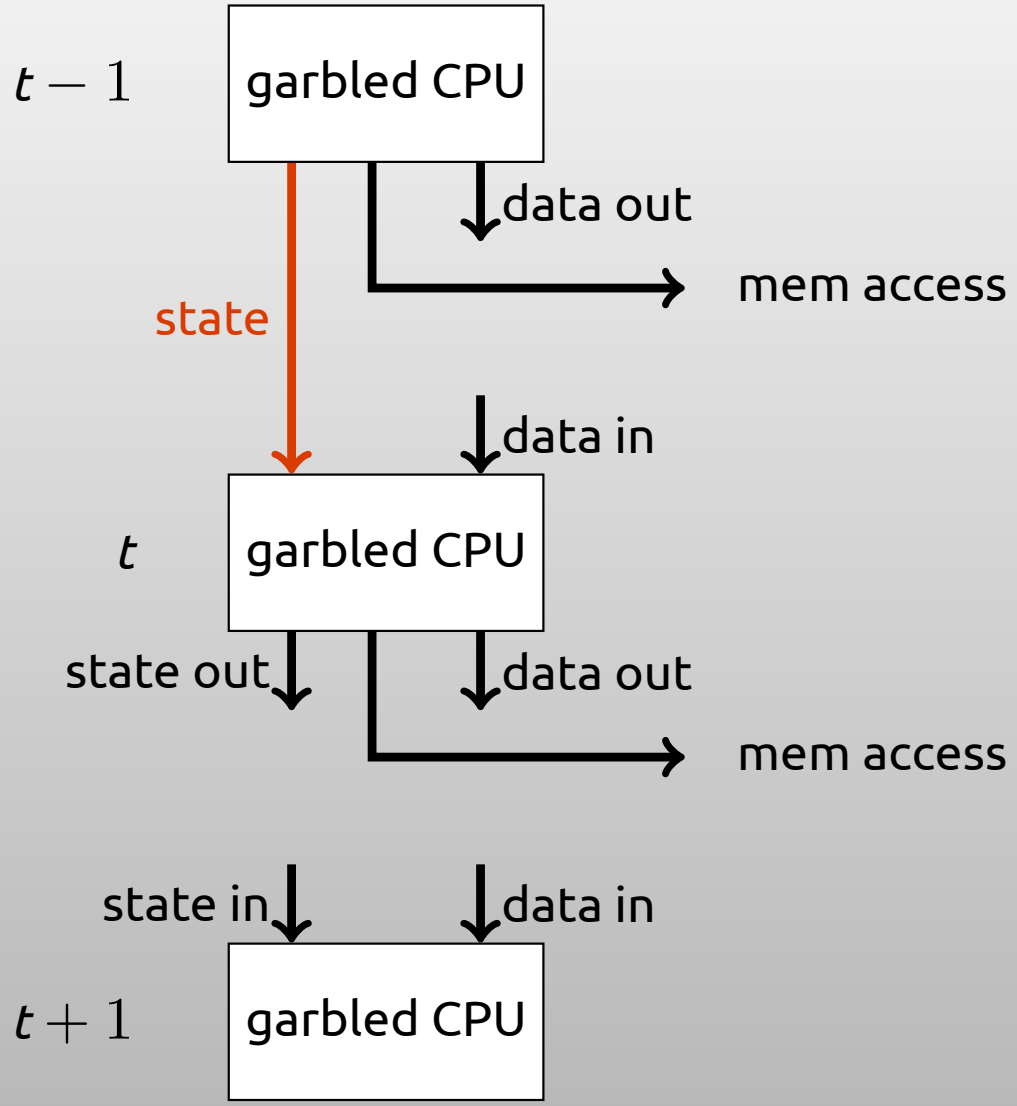

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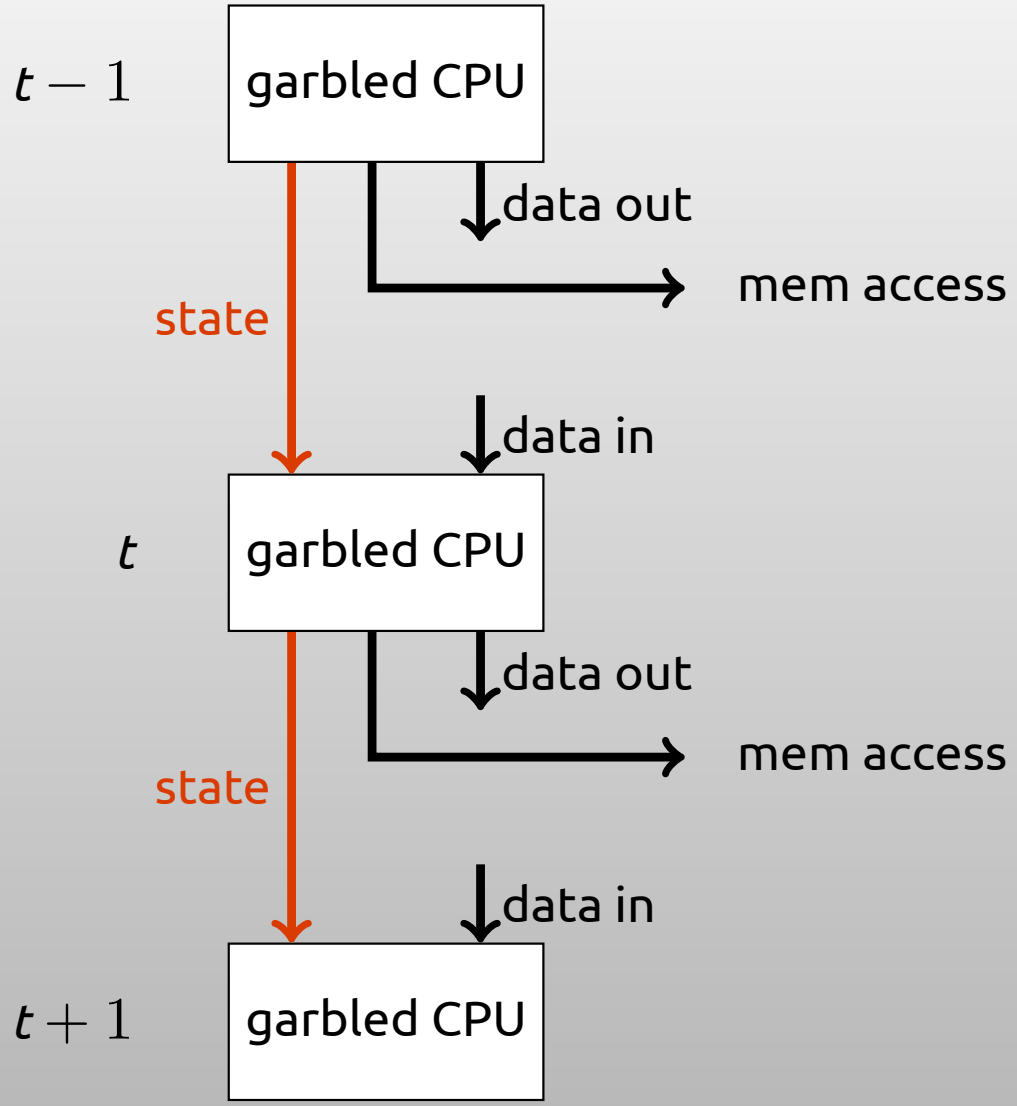

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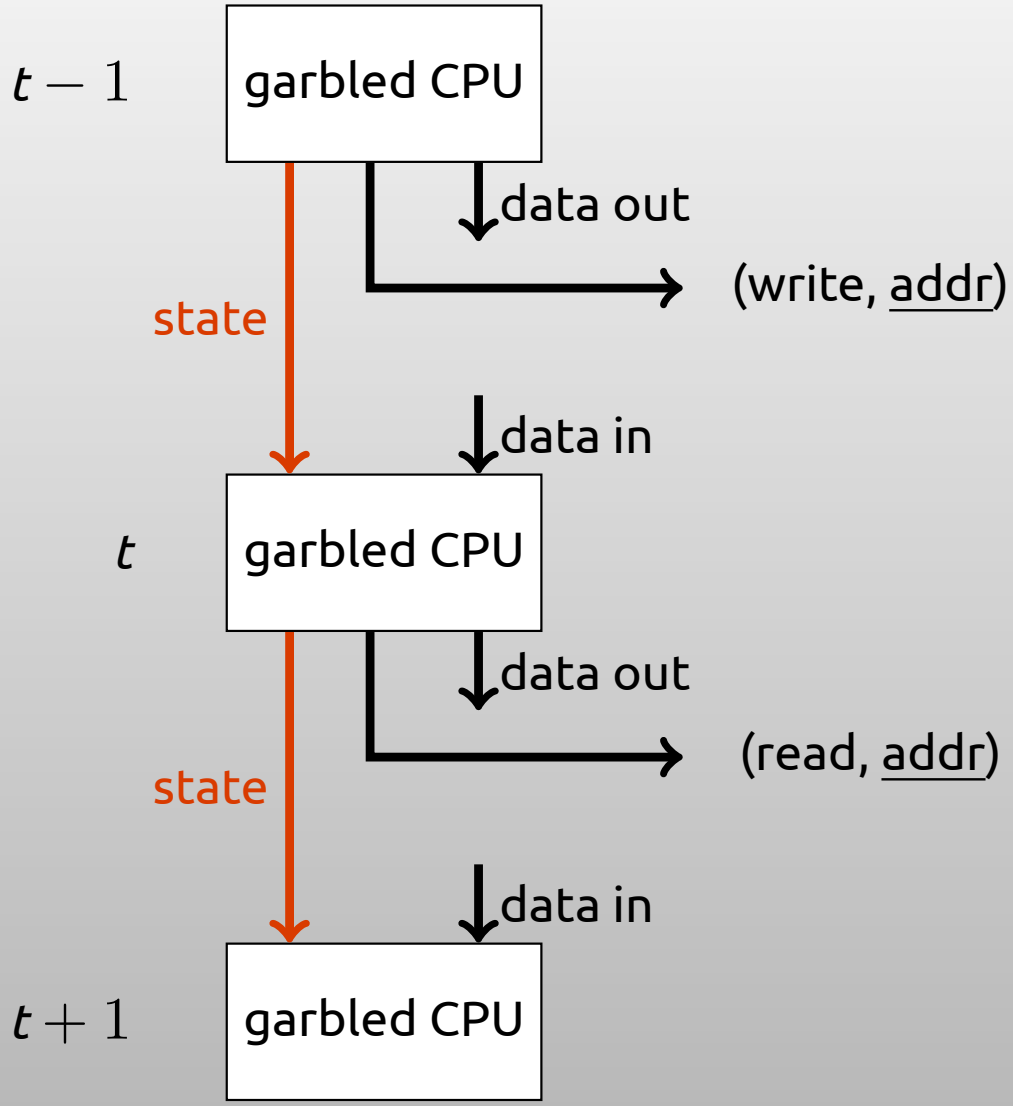

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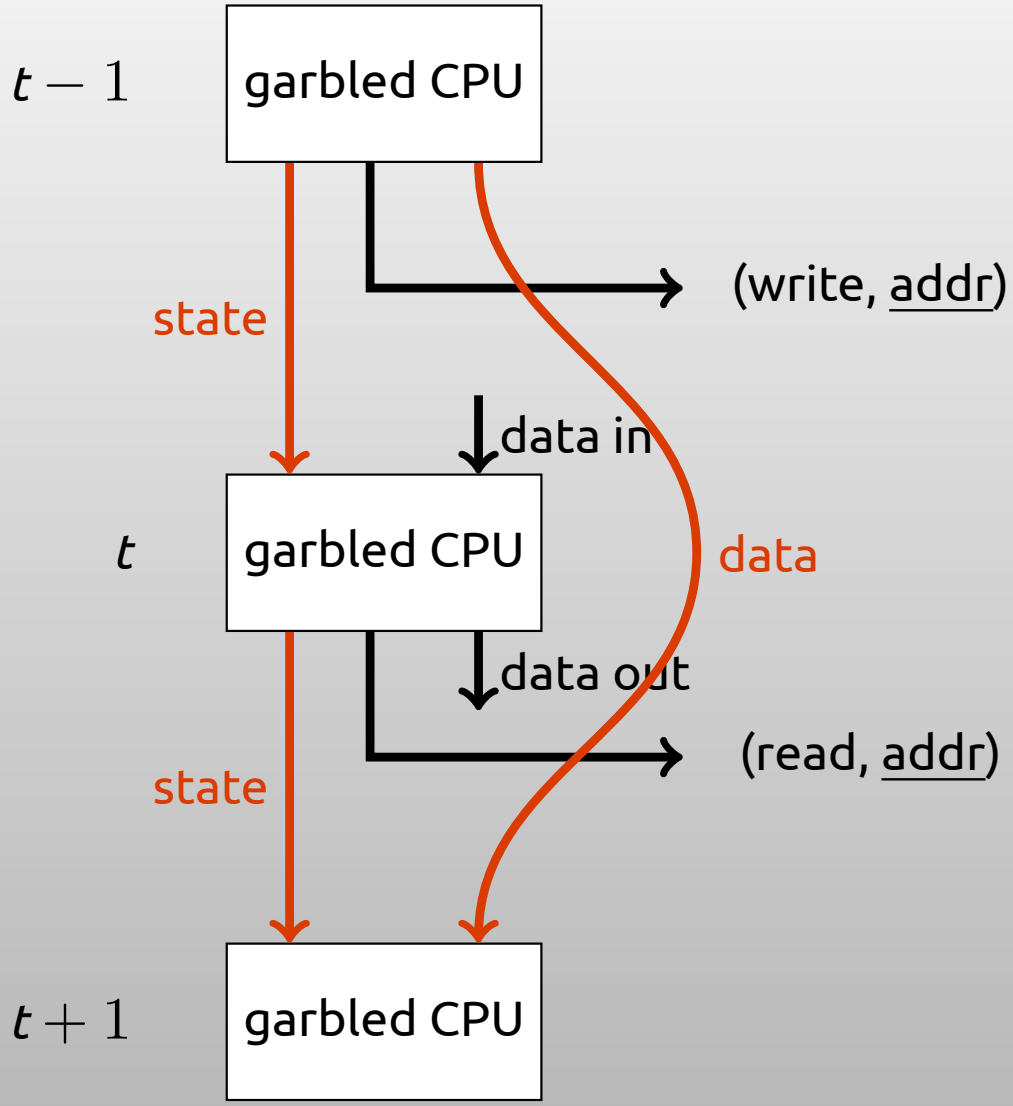

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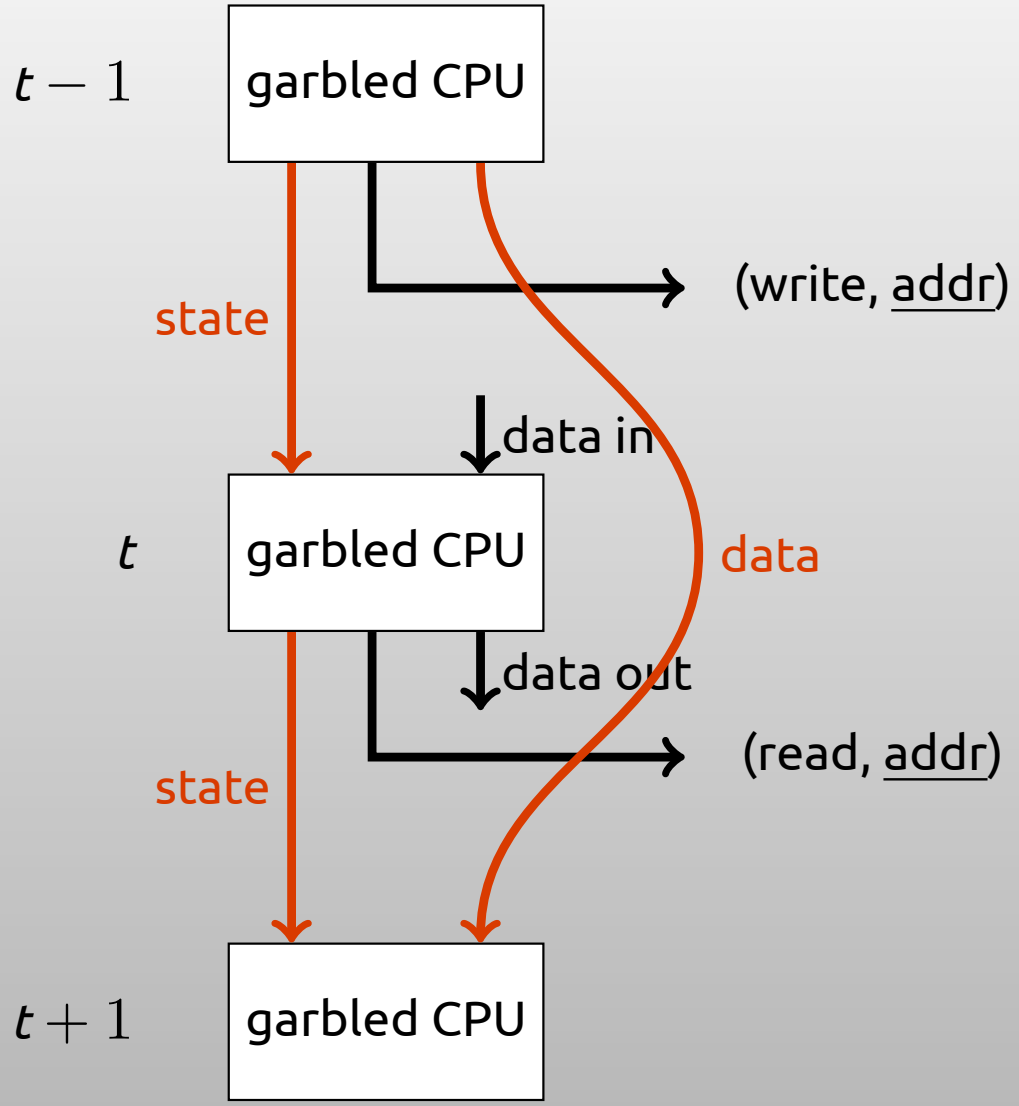
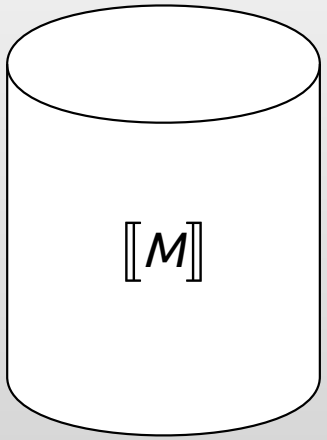


Must know ORAM access pattern to choose appropriate garbled encoding for next circuit.

(Contrast with naively converting ORAM to circuit)

Our approach [AfsharHuMohasselR15]



⟦state⟧

- Memory and state encoded with garbled encoding.

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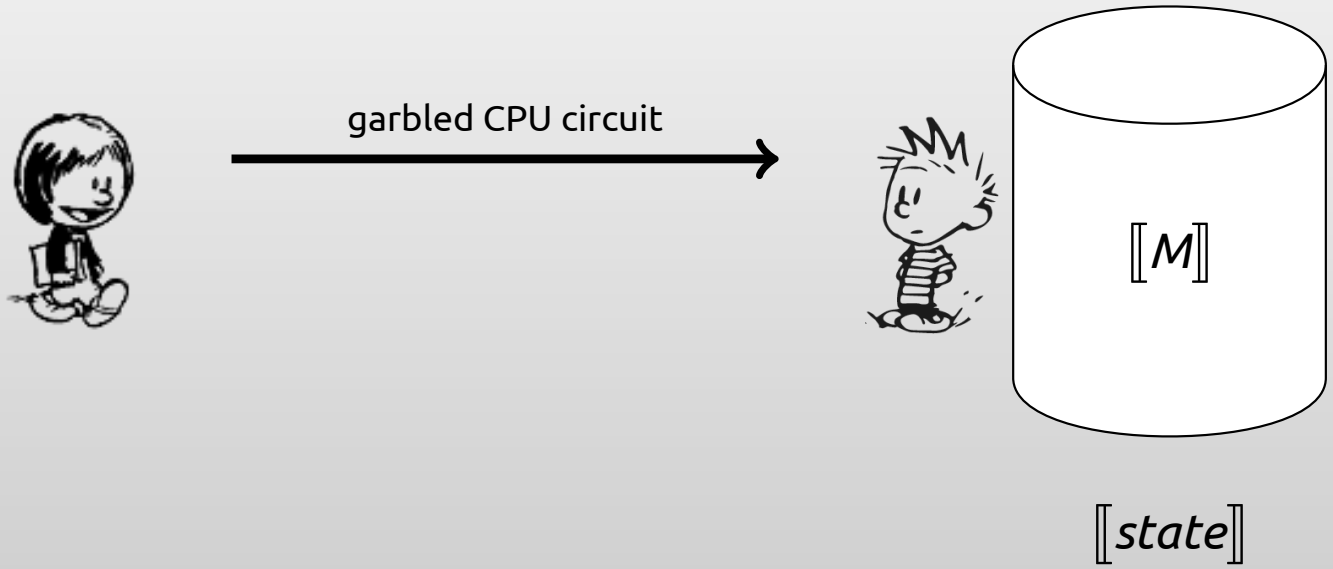

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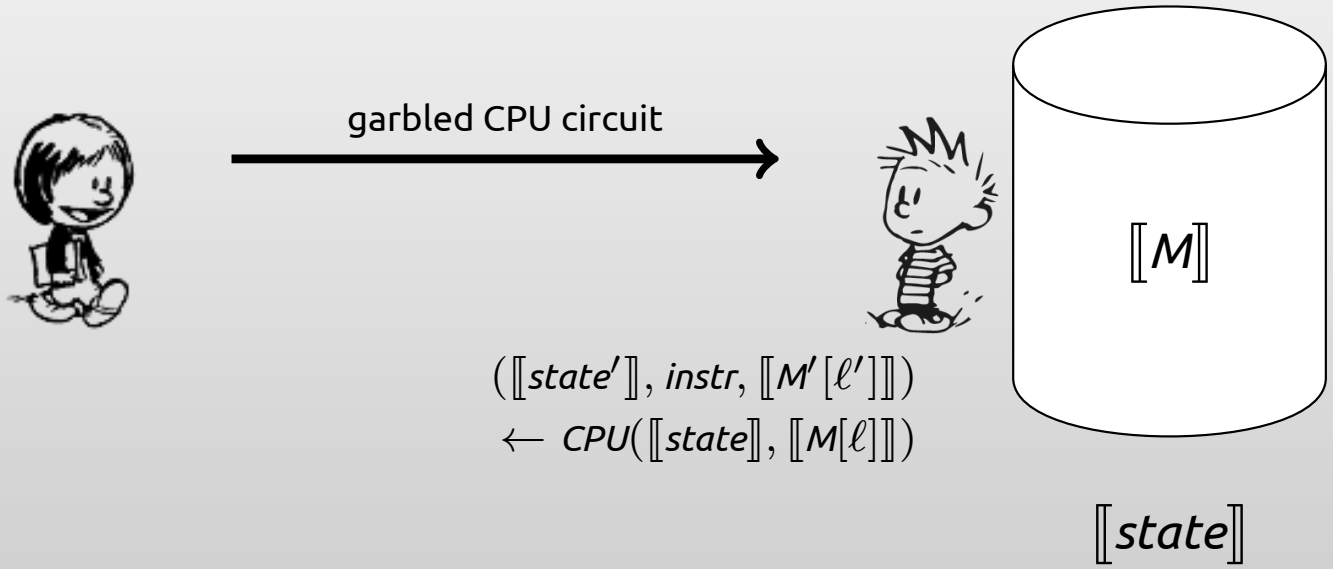

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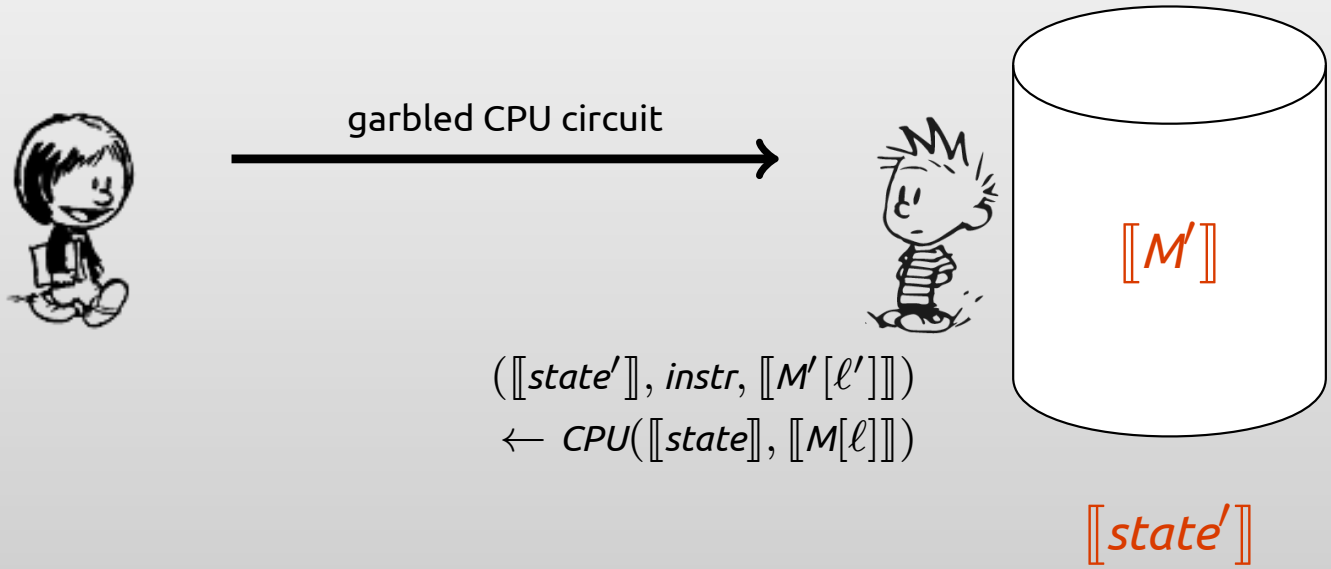

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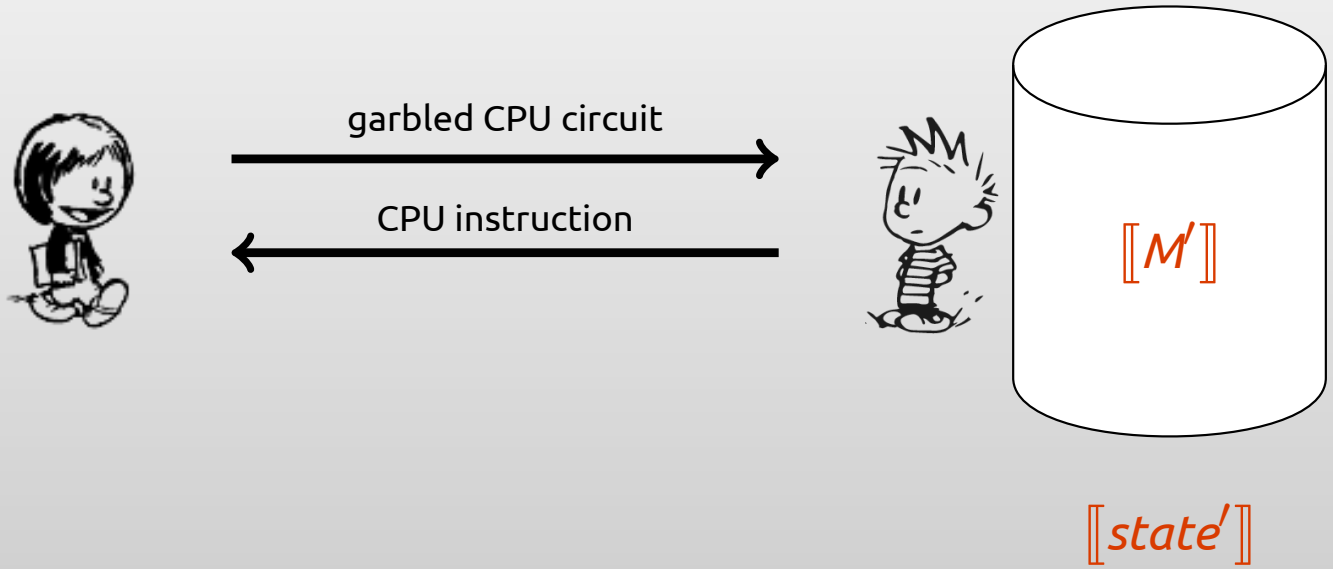

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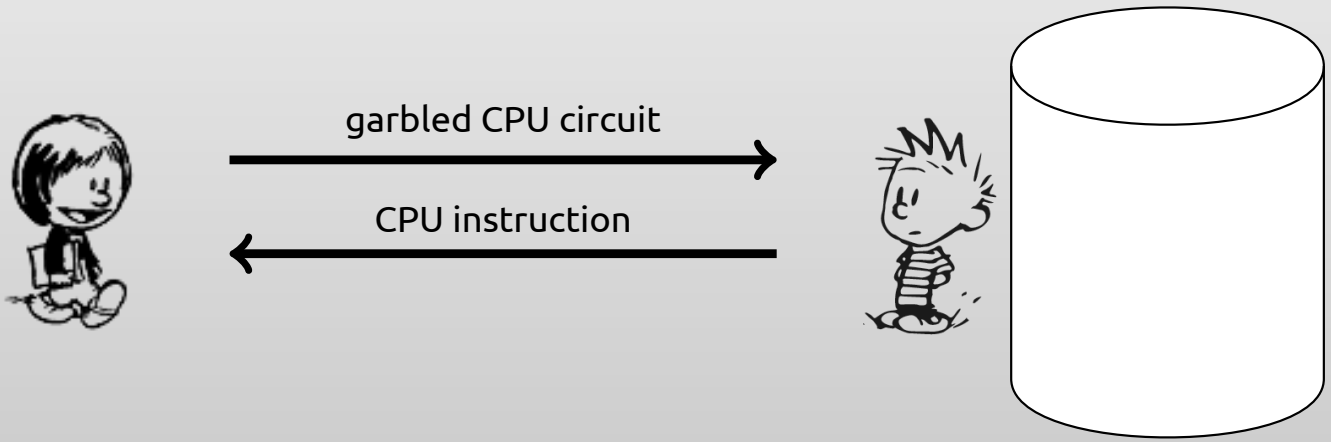
Malicious garbler



Main challenge: malicious garbler generates invalid garbled circuits.

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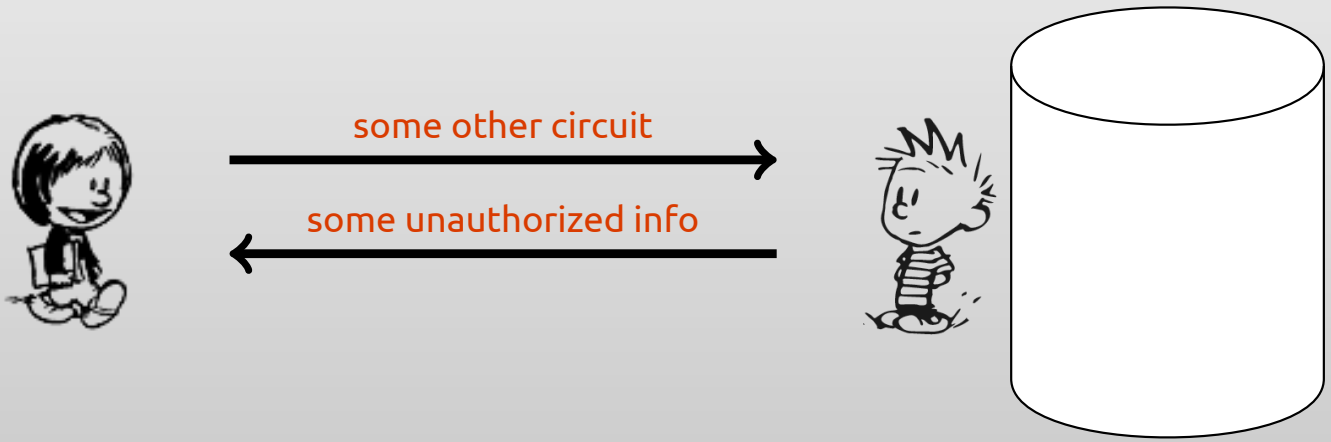

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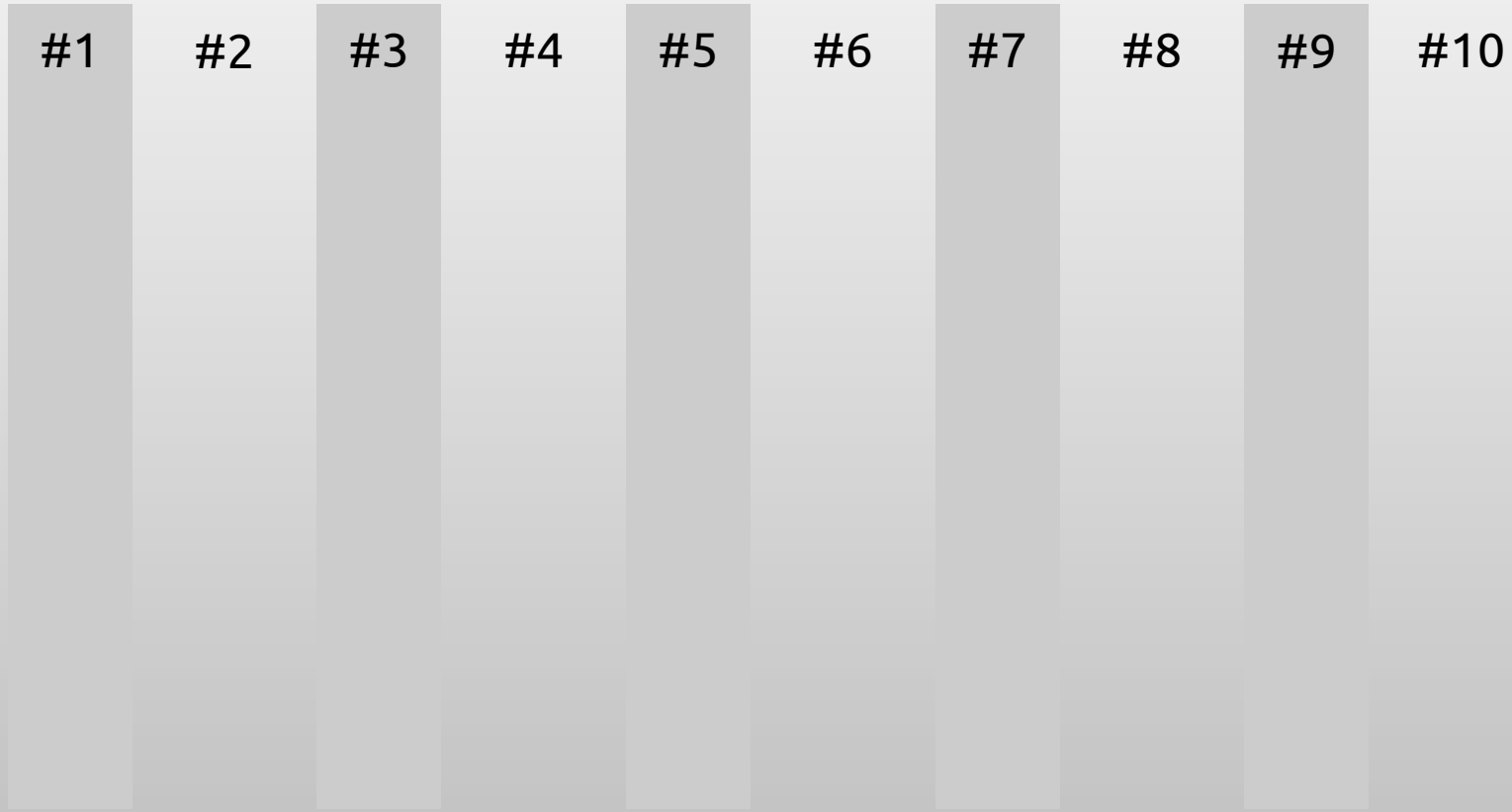
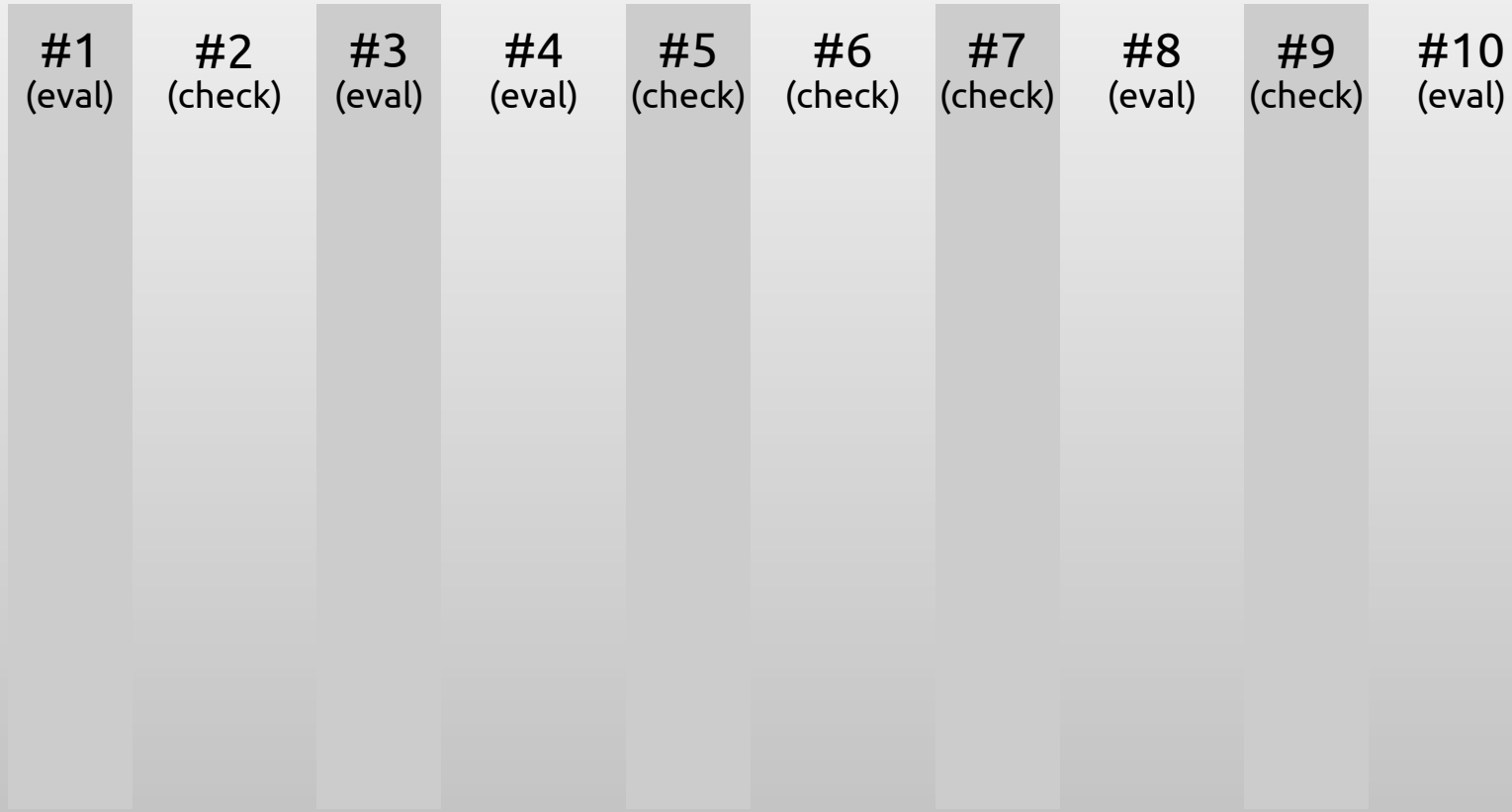


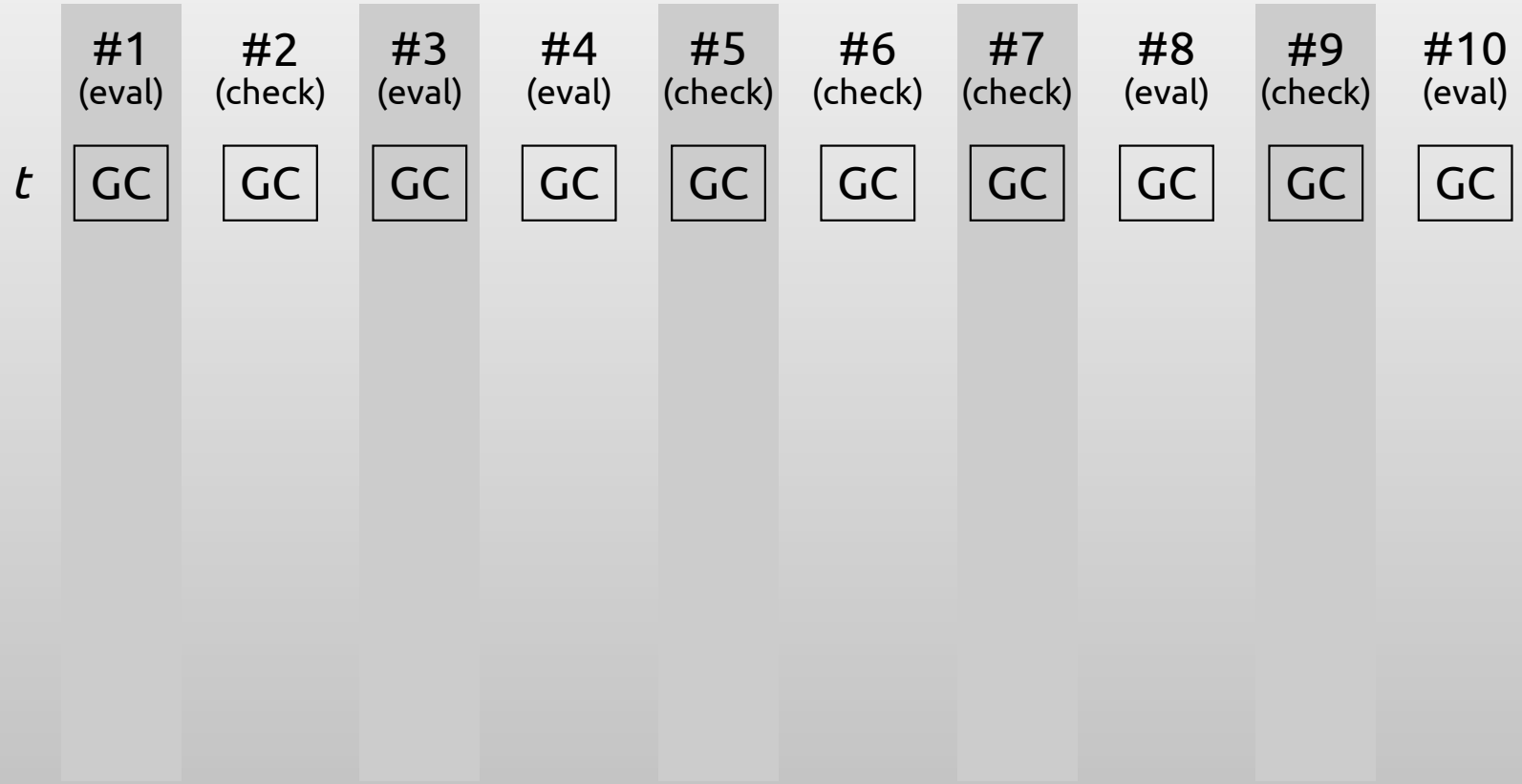
establish many threads of computation

cut and choose



receiver secretly sets each thread to “check” or “eval”

cut and choose



sender generates garbled circuits, reusing wire labels within each thread

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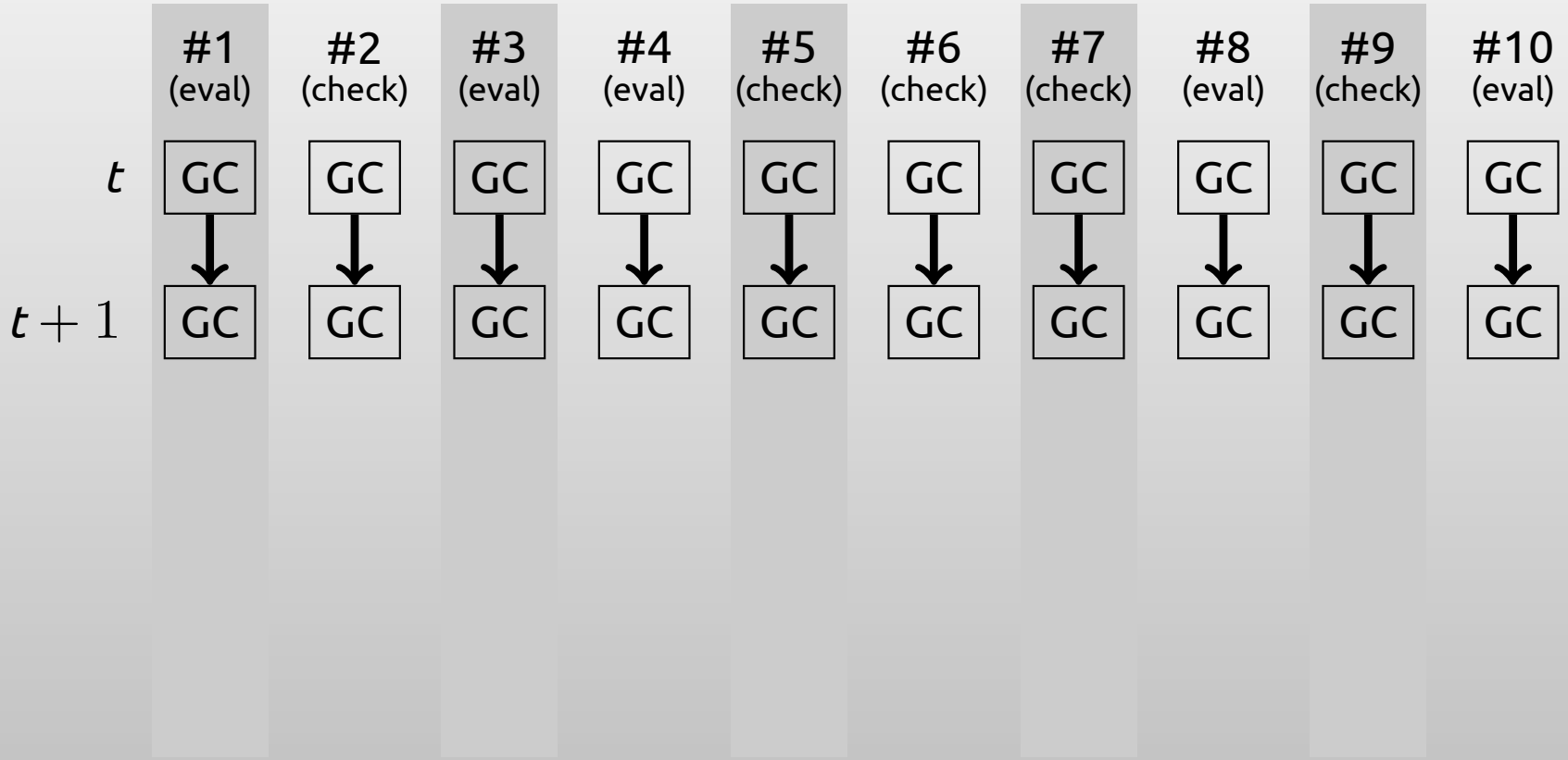

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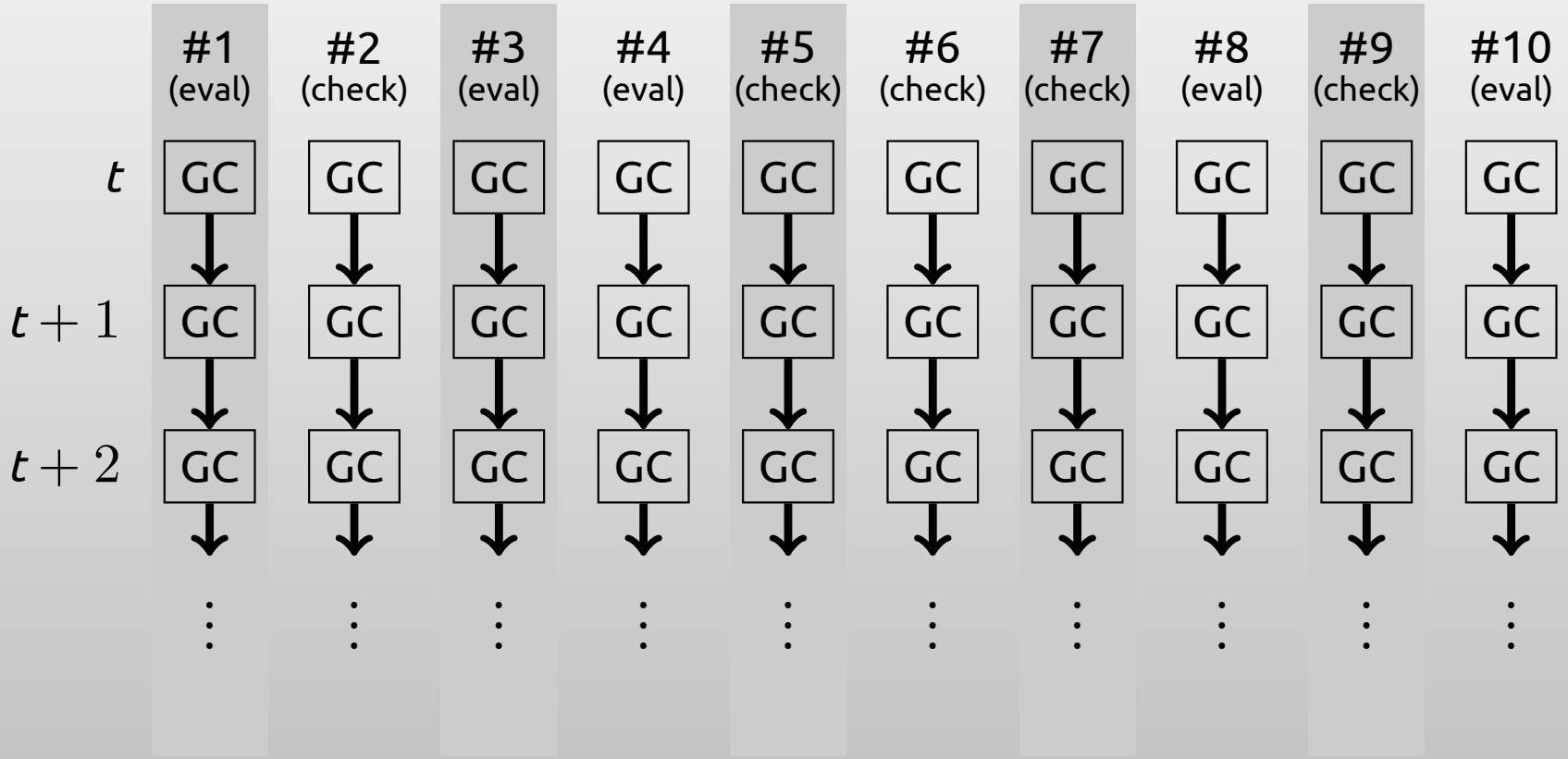

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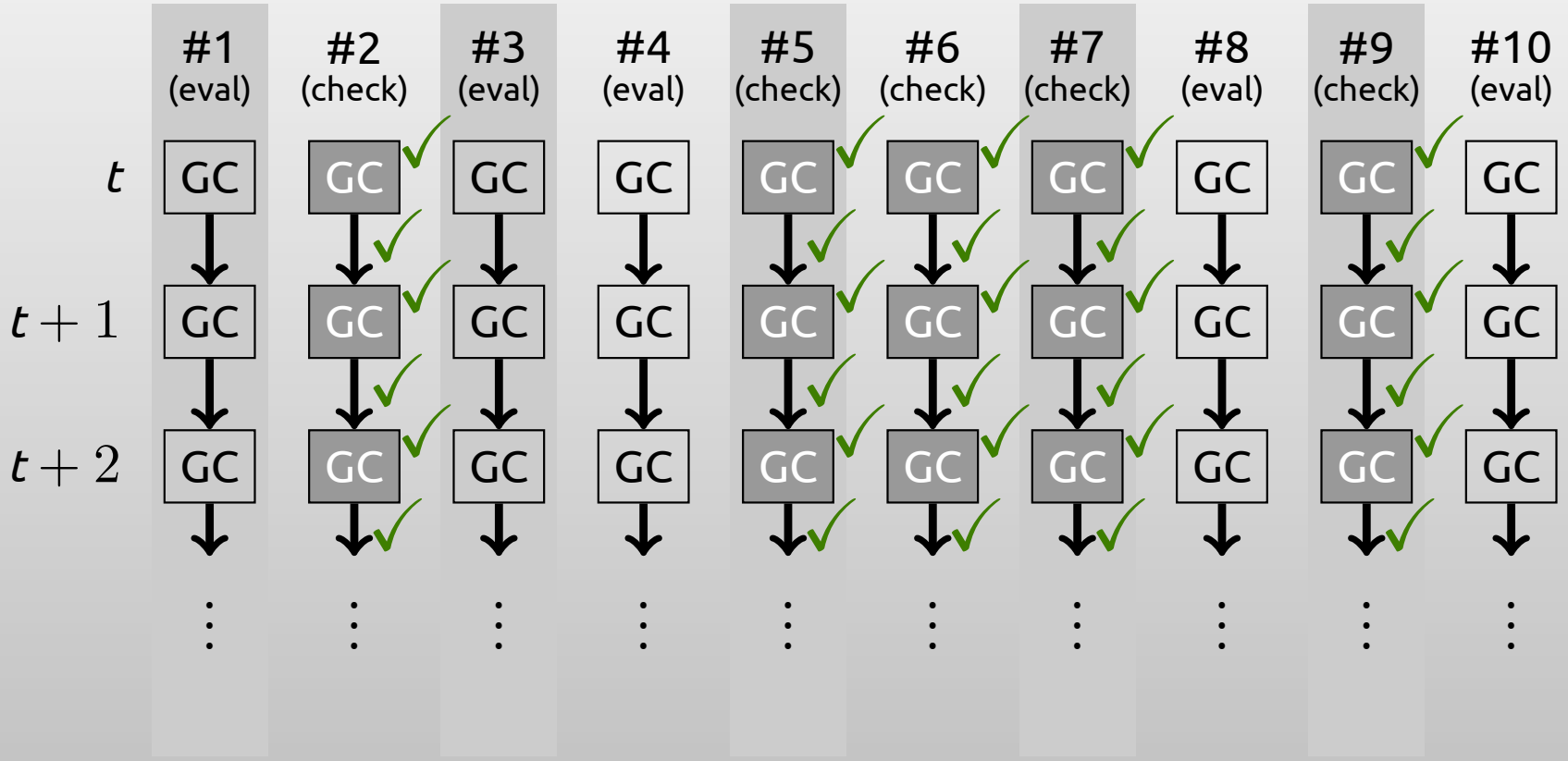

check-threads: receiver gets both labels per wire $\Rightarrow$ check correct behavior

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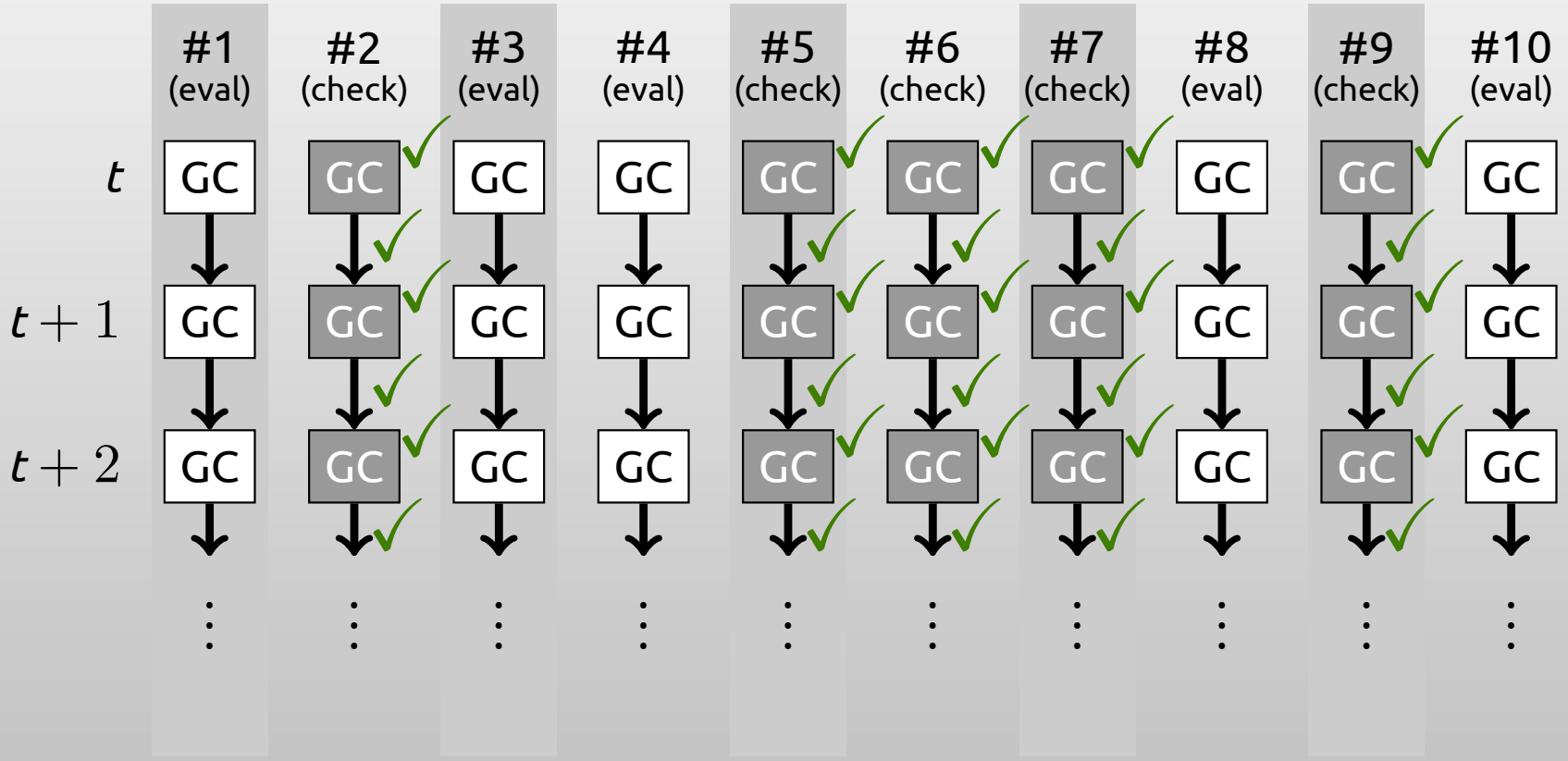
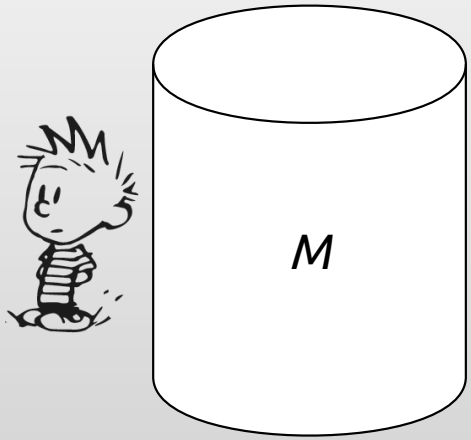


eval-threads: receiver gets one garbled encoding $\Rightarrow$ learns only prescribed outpu

One-sided secrets



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- *M* is Calvin's secret input; expensive ORAM initialization commits him to *M*
- Repeatedly run *public* ORAM program on *M*
- Example: *M* = user database; check for membership

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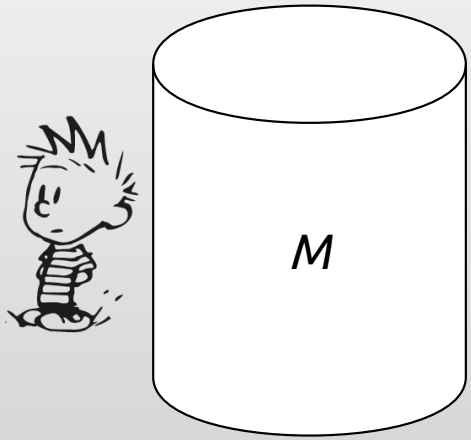

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In this case we can avoid cut & choose, avoid high interaction!

Avoiding cut and choose [HuMohasselR15]

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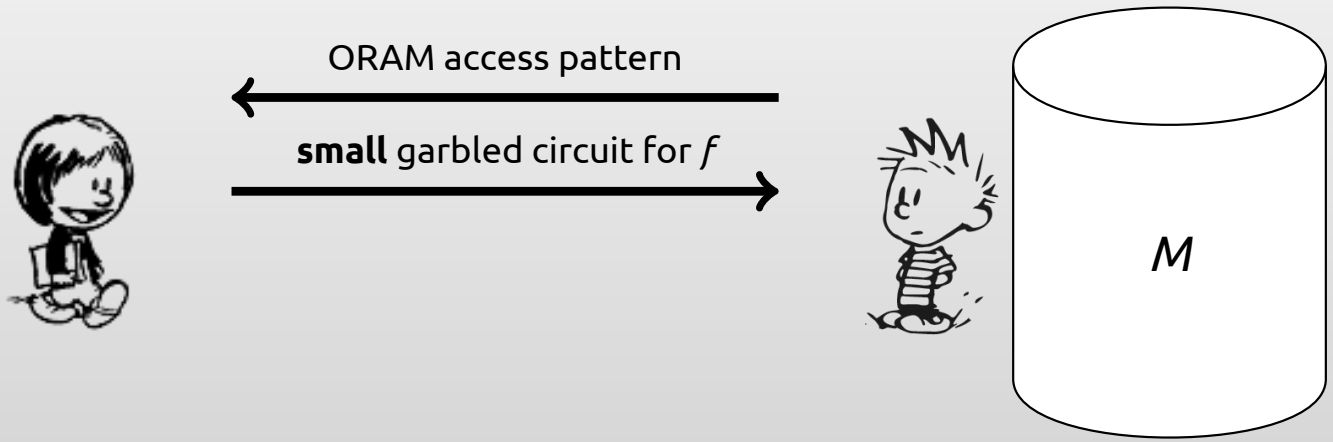

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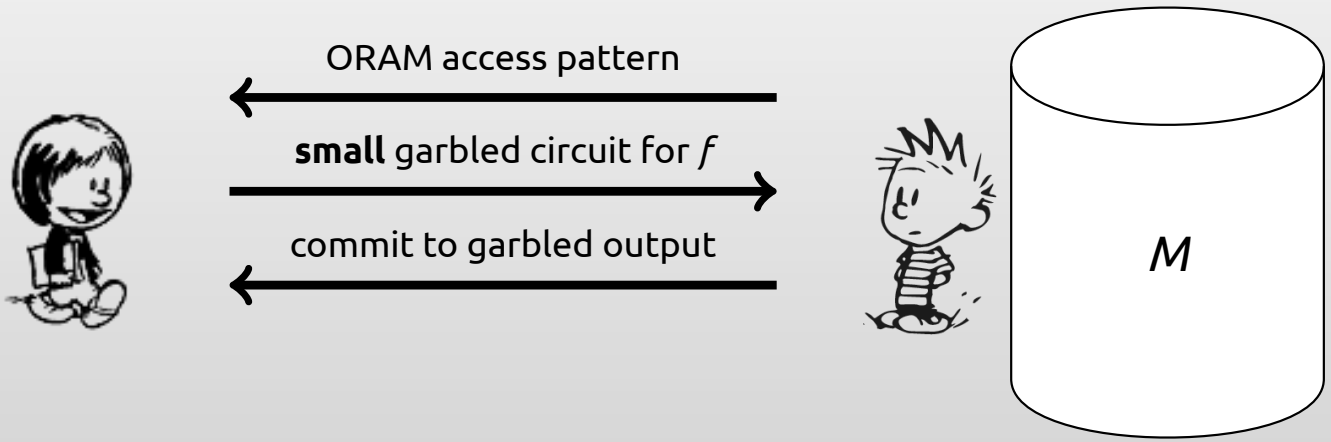

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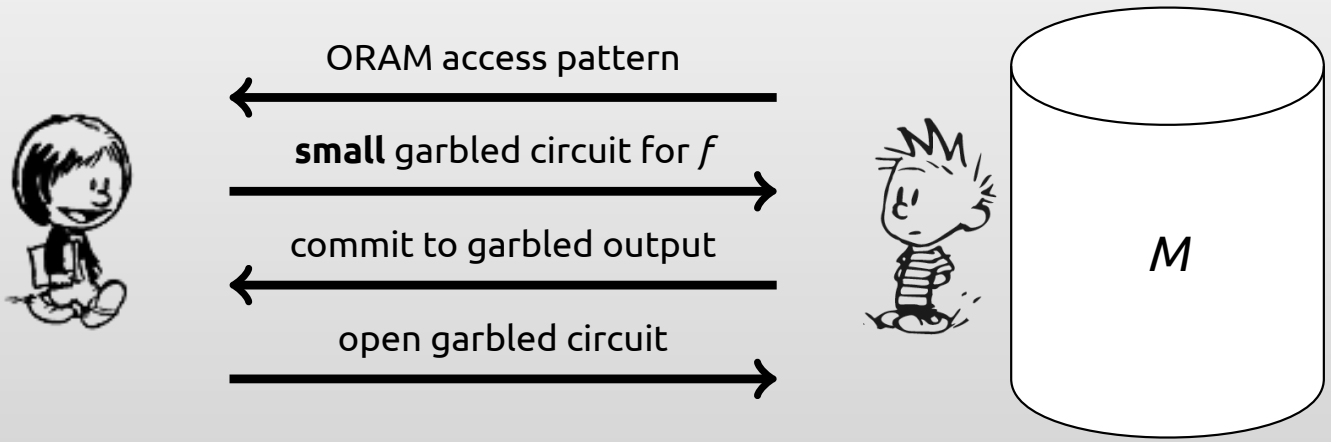

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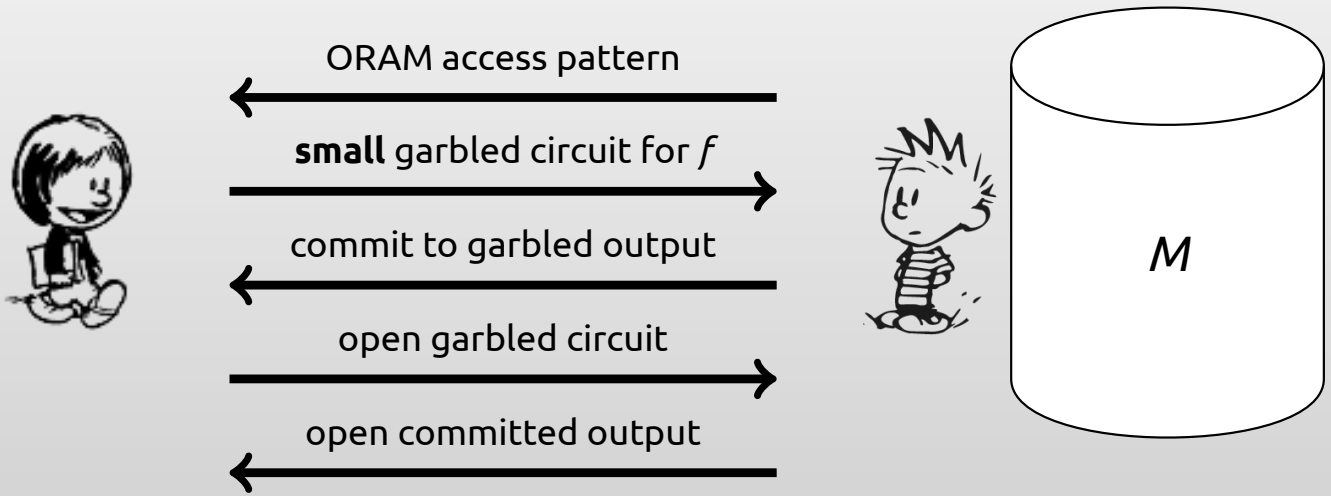

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Conclusion

RAM-based 2PC can provide sublinear cost in **amortized sense**, using practical 2PC techniques

- [GKKKRV12] = general paradigm, semi-honest security
- [AHMR15] = malicious security
- [HMR15] = malicious security with one-sided secrets; no cut-and-choose, constant rounds

Challenges:

- Expensive pre-processing (ORAM initialization): communication & computation
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